

EXHIBIT 24-A

EXHIBIT 24-B

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ENDBATES	QCARM_2541343
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NATIVEPATH	

EXHIBIT 25

**IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE**

ARM LTD., a U.K. corporation,
Plaintiff,

v.

QUALCOMM INC., a Delaware
corporation, QUALCOMM
TECHNOLOGIES, INC., a
Delaware corporation, and NUVIA,
INC., a Delaware corporation,
Defendants.

C.A. No. 22-1146 (MN)

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ONLY**

OPENING EXPERT REPORT OF DR. ROBERT P. COLWELL

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I. INTRODUCTION

1. My name is Dr. Robert P. Colwell, and I have been retained as an expert witness on behalf of the Plaintiff Arm Ltd. in this matter. I understand that Arm has sued Defendants Qualcomm Inc., Qualcomm Technologies, Inc., and Nuvia, Inc. in the District of Delaware in the case captioned *Arm Ltd. v. Qualcomm Inc. et al.*, No. 1-22-cv-001146-MN (D. Del.). I am being compensated for my time in connection with this proceeding at \$650/hour. My compensation is not dependent on the substance of my opinions, my testimony, or the outcome of this proceeding.

2. I have been asked to analyze whether certain Qualcomm CPU cores incorporate technology developed by Nuvia under the Nuvia Architecture License Agreement (“Nuvia ALA”), [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

3. As discussed further below, it is my opinion that:

(i) The [REDACTED] core initially developed by Nuvia (a) was designed to be

[REDACTED]

[REDACTED] (b) implements the Arm instruction set and other components of

[REDACTED]; and (c) was validated as an

Arm [REDACTED].

(ii) Qualcomm incorporated substantial parts of the Nuvia-designed [REDACTED]

core into later versions of the [REDACTED] core used in certain Qualcomm

System-on-Chip (“SoC”) products, including the [REDACTED] core, the [REDACTED] core, and the [REDACTED] core.

(iii) While I understand that Qualcomm claims it swapped out certain Arm IPs from its products following Arm’s termination of the Nuvia licenses, the documents and testimony provided by Qualcomm indicate that [REDACTED]

[REDACTED]

[REDACTED]

4. I base my opinions on my extensive experience in the industry; experience with Arm technology; my review of documents produced in this litigation; my review of deposition transcripts; my review of discovery responses; a conversation I had with Arm Chief Architect Richard Grisenthwaite on December 13, 2023; source code produced by Qualcomm; and other materials. I also reviewed the Expert Report of Dr. Shuo-Wei (Mike) Chen submitted in this case. I include a list of materials considered in Appendix A to this report.

II. EXPERIENCE AND QUALIFICATIONS

5. I am a technical expert in the field of computer engineering and microprocessor design. I am also an industry expert in those fields. I attach a copy of my *curriculum vitae* as Appendix B to this report, which describes my relevant experience, including academic and employment history, publications, professional activities, and speaking engagements.

6. I received a B.S. degree in Electrical Engineering from the University of Pittsburgh in 1977. I received an M.S. degree in Computer

Engineering from Carnegie Mellon University (CMU) in 1978, followed by a Ph.D. in Computer Engineering from CMU in 1985.

7. From 1977 until 1980 I worked for Bell Laboratories in Holmdel, New Jersey as a hardware design engineer developing 8- and 32-bit microprocessors. My specific responsibilities included design and support of their in-circuit emulators, and design and timing analysis of interchip signaling protocols.

8. From 1980 until 1984, while obtaining my Ph.D., I worked part time for Perq Systems in Pittsburgh, Pennsylvania, as a hardware design engineer working on high-resolution graphics display hardware for first generation bit-slice-based workstations.

9. From 1985 until 1990, I worked at Multiflow Computer in Branford, Connecticut, as a hardware design engineer creating the world's first VLIW (very long instruction word) scientific supercomputer. Multiflow sold about 125 such systems at an average selling price of \$200K.

10. From 1990 to 2001, I held various positions at Intel Corp. in Hillsboro, Oregon, including Senior CPU Architect and Chief Architect (for Intel's IA-32, also known as x86). As part of my responsibilities at Intel, I co-invented Intel's P6 microarchitecture, productized as the Pentium Pro, which also formed the core of the Pentium II, the Pentium III, Celeron, Xeon, and Centrino families, as well as the Pentium 4. P6 microarchitecture features are still very influential today in Intel's top-of-the-line Core i3, i5, i7,

i9, and X-series processors. In addition, I led Intel's overall x86 Pentium CPU architecture endeavors across multiple chip developments. I was honored to be named an Intel fellow in 1997 in recognition of my contributions to the P6 microarchitecture development. Overall, I worked with and spent 11 years leading a large industrial microprocessor design team at Intel, which by the late 1990s included more than 850 engineers.

11. Along with the x86 chip development work, in my role as Intel's Chief Architect, I also tracked current and emerging competition in the microprocessor product space. Although Arm Inc. products were not performance-competitive with Intel's chips in the 1990's, I paid attention to Arm because my personal conviction in the late 1990's was that low-power and low-cost processors would increasingly be required in the future mobile computing platforms that I was sure would emerge (which turned out to primarily take the form of smartphones and tablets). I analyzed the ARM instruction set, core performance, and software tool availability (compilers, debuggers, simulators), as well as projected licensing costs and support models. The conclusion I reached at the time, and still hold today, is that a capable design team could use the ARM instruction set to design Arm-compliant processors that would challenge the best processors from Intel

or AMD in every market segment. My conclusion ended up being correct, as evidenced by Apple's introduction of the M-series processors.¹

12. While at Intel, I also paid attention to Qualcomm, because I found it worrisome that we at Intel had a processor product line that had little to offer the coming mobile computing markets. Intel had no suitable x86 cores to sell to those low-power markets, and no ability to license x86 cores to Qualcomm, even if we had those cores in our product line. Given Qualcomm's long history in the cell phone industry, which is necessarily a mobile and battery-operated environment, the SoC paradigm looked to be a natural fit to serve as the basis for those mobile products. SoCs are space-efficient, incorporating most of the necessary system functions on a single chip, and power-efficient because electrical interconnections are short and the SoC designers can optimize the SoCs' functions rather than having to use whatever is available. SoCs require, among other things, one or more CPUs, each with one or more processor cores. Licensing cores from a company dedicated to developing those cores is an effective solution compared to creating and permanently maintaining a CPU core development team so that each new generation remains performance competitive.

13. I became a self-employed industry consultant in 2001, working with computer industry clients such as Safeware, the University of

¹ Hassan Mujtaba, *Apple M1 ARM 8 Core CPU Is Faster Than Intel & AMD's Fastest 8 Core Chips in Single-Core Performance Benchmark*, WCCFTECH (March 25, 2021), <https://wccfttech.com/apple-m1-arm-8-core-cpu-faster-intel-amd-fastest-8-core-chips-single-core-performance/> (last visited December 19, 2023).

Pittsburgh, Intel, venture capital companies, various expert witness engagements, and the U.S. Department of Defense (DoD).

14. In 2011, I joined DoD's Defense Advanced Research Projects Agency (DARPA) as deputy director of the Microsystems Technology Office (MTO). DARPA is the U.S. government's premier defense-related funding agency, specializing in high-risk and high-reward technologies for the U.S. military. A year later I became MTO's director, until my departure in April 2014. MTO had an annual budget of approximately \$600M, and my job as office leader was to invest that money in promising new technologies for the DoD, including new energy-efficient computing systems, modular and adaptable radars, position/navigation/timing systems for GPS-denied environments, computer-mediated prosthetics for military (and civilian) amputees, traumatic brain injury detection devices for soldiers, fused multiple-band night vision sensors, extremely high-power lasers, and much more.

15. I have authored numerous publications including books, chapters in books, journal papers, and numerous patents (40) associated with computer hardware and processor design. My *curriculum vitae* includes a list of all the publications I have authored in the last 10 years. Many of these publications concern the design of microprocessors and computer systems. I have also been an editor for Institute of Electrical and Electronics Engineers (IEEE) publications, as well as a columnist and author.

16. I have received multiple awards, including the 2005 Eckert-Mauchly Award for “outstanding achievements in the design and implementation of industry-changing microarchitectures.” The Eckert-Mauchly Award is generally viewed as the highest recognition in the field of computer architecture. In 2006, I was elected to IEEE Fellow and inducted into the National Academy of Engineering for contributions to turning novel computer architecture concepts into viable, cutting-edge commercial processors. In 2012, I was inducted into the American Academy of Arts and Sciences (AAAS). Other inductees in my AAAS “class” that year included Sir Paul McCartney, Hillary Rodham Clinton, and Mel Brooks. In 2015, I received the Bob Rau Award from the IEEE for “contributions to critical analysis of microarchitecture and the development of the Pentium Pro processor.”

III. BACKGROUND AND OPINIONS

A. Microprocessor Industry

17. A microprocessor is a computer on an integrated circuit, also known colloquially as a “computer chip.” The “micro” part of the word “microprocessor” refers to the physical size of the processor. At the time the term microprocessor was coined (1971), computer systems were the size of several full-sized refrigerators, while the microprocessor was the size of a pack of chewing gum. Regardless of size, all such processors can fetch and execute machine instructions from main memory. A microprocessor is also known as a “CPU,” or Central Processing Unit. A new term for

microprocessors, “core,” has come into vogue since the burgeoning number of transistors afforded by Moore’s Law enabled the industry to put more than one CPU onto a single integrated circuit. By convention, the product is still called a microprocessor, but there can be multiple cores within that processor, each capable of independently fetching and executing its own instruction stream. These multiple independent cores may share certain facilities such as a common cache, an on-chip network, access to main memory, and an input/output interface.

18. Other components of a modern computer system, such as those in a smartphone, can also be integrated onto the same silicon as the cores, yielding a product conventionally called a System-on-Chip, or SoC.

19. Microprocessors and SoCs are now ubiquitous in everyday life and are no longer found just in computer systems, phones, and tablets. Modern automobiles have many different processors, from entertainment systems, security systems, engine controllers, antilock brake controllers, transmission controllers, to the key fob that opens the doors. Likewise, today’s homes are rife with computing horsepower: processors run the microwave, washing machine, dryer, furnace, TV, router, cable modem, and even light switches and flashlights.

20. The International Trade Commission (ITC) estimates the size of the global information technology (IT) sector to be \$5T and more than 10% of

the U.S. gross domestic product.² Several of the largest companies in the world are heavily IT-centric. By some metrics, Apple is #1 with the largest market cap at \$2.65T. Microsoft is #3 with a market cap of \$2.1T, Alphabet (Google) at #4 with \$1.54T, Amazon at #5 with \$1.42T, NVIDIA with \$1.06T, Tesla at #6 with \$910B. By contrast, Toyota, a more conventional manufacturing company, has a market cap of \$236B. The entire U.S. movie industry revenue in 2022 was \$41.7B, and the music industry at \$19.1B in 2020, while the high-tech video game market was valued at \$159.3B in 2020, three times higher than movies and music combined.³

21. It is important to realize that new computer technology does not just afford incremental improvements to existing products or markets, but also enables entirely new markets and products. For instance, the Internet came into existence when computers became fast enough, and inexpensive enough, to handle the data traffic. Smartphones became feasible products when processors became fast enough to execute useful applications at power levels that did not quickly drain the battery.

² David Coffin et al., *The Roadblocks of the COVID-19 Pandemic in the U.S. Automotive Industry*, U.S. INTERNATIONAL TRADE COMMISSION (USITC) (June 2022), https://www.usitc.gov/publications/332/working_papers/the_roadblocks_of_the_covid-19_pandemic_in_the_automotive_industry_final.pdf (last visited December 19, 2023).

³ Gavin Divers, *Gaming Industry Dominates as the Highest-Grossing Entertainment Industry*, GAMERHUB (January 24, 2023), <https://gamerhub.co.uk/gaming-industry-dominates-as-the-highest-grossing-entertainment-industry/#:~:text=To%20put%20that%20in%20perspective,much%20as%20the%20movie%20industry> (last visited December 15, 2023).

2. Microprocessor Architectures.

22. A computer instruction set architecture (ISA) is the list of instructions that a compatible processor is able to execute, plus other information needed by an assembly language programmer, such as the number and width of the machine's registers, addressing modes, control register descriptions, supported data types (*e.g.*, integers, single and double precision floating point, and strings), as well as the actual bit-for-bit encoding of the instructions.

23. A computer instruction is an operation that a given processor “knows how to perform,” encoded into a pattern of bits that the processor can decode and execute. A canonical example might be an integer add instruction. For the Arm ISA, the corresponding “opcode” would be called ADD, and the overall instruction would specify the two source registers whose contents are to be added together, plus a destination register indicating where the sum is to be written. If the data to be added happened to reside in main memory, two memory loads would have to first be performed to get the data into the registers. The much more complicated Intel x86 architecture, by contrast, allows the ADD instruction itself to access memory for one of the source values, and the destination can also be memory.

24. ISAs such as Intel's x86 architecture comprise hundreds (or thousands, depending on how one counts) of instructions, which include simple instructions but also much more complicated operations that require microcode (a kind of computer-within-the-computer code) for their

implementation. This type of ISA is known as complex instruction set computers (CISC).

25. Originally, Arm's ISA had only a few dozen instructions and adhered to a design philosophy known as reduced instruction set computers (RISC). Subsequently, the Arm ISA has added several hundred more instructions with Armv8. The Arm ISA can directly access 16 registers from user mode, while the x86 architecture has only 4 such registers, with a few others that are dedicated to certain activities, plus some vestigial segment registers. Arm has two operating modes, user and privileged, while x86 has a more elaborate ring mechanism.

26. Below is a screenshot of a few exemplary instructions from the Arm A64 Instruction Set (described in the Arm ARM), including the ADD instruction previously discussed. The ADD instruction, as discussed above, simply adds two data values together and puts the sum into a destination register. (The "immediate" tag on these particular instructions signifies that one of the data values to be added is not in a register but is contained within the instruction encoding itself, making it "immediately" available to the hardware adder.) The ADDS instruction does exactly the same operation as ADD, but also sets some one-bit result (also called "status") flags such as Zero, Negative, Carry, and Overflow. The SUB and SUBS instructions are just like ADD/ADDS except that they perform subtraction instead of addition. Compare instructions set the result flags according to whether one data value

is larger or smaller than the other one, and the result flags are generally used by subsequent conditional branches.

Table C3-42 Arithmetic instructions with an immediate		
Mnemonic	Instruction	See
ADD	Add	<i>ADD (immediate)</i> on page C6-883
ADDS	Add and set flags	<i>ADDS (immediate)</i> on page C6-891
SUB	Subtract	<i>SUB (immediate)</i> on page C6-1455
SUBS	Subtract and set flags	<i>SUBS (immediate)</i> on page C6-1466
CMP	Compare	<i>CMP (immediate)</i> on page C6-982
CMN	Compare negative	<i>CMN (immediate)</i> on page C6-976

Figure 1: Arithmetic Instructions from Arm A64 Instruction Set. (ARM_01324149 at -390.)

27. The Intel x86 ISA evolved largely as a competition between one generation of CPUs and the next generation – if a new Intel chip was not compellingly faster than the existing one, the new one would not command a profit margin high enough to underwrite the next generation of fab equipment. While Intel chip designers still had to balance multiple competing factors in creating a new chip, such as performance, power dissipation, product cost, schedule, and risk of design errata, performance generally came first among design goals. It was my experience that the last 10% of performance gain in a design comes at a disproportionately large cost in power and design effort. The Arm ISA, by contrast, explicitly aimed to enable compatible implementations that emphasized good performance at

outstanding power efficiency, an excellent recipe for the computational elements underlying smartphones and tablets.

28. Developing a new ISA requires achieving a subtle and extremely complex balance among many competing concerns. Beyond a minimal set of instructions that any ISA would be expected to have (integer ADD, for example), designers could choose to add more instructions, attempting to provide hardware to support high-level functions in the user code for best performance. But it can be difficult for a compiler to spot opportunities to use those specialized instructions, and meanwhile, the bit encodings of the instructions will be necessarily larger, thus potentially compromising other aspects of the machine, such as cache performance. It is also quite easy to (intentionally or otherwise) embed certain aspects of the current microarchitecture into the ISA itself, which then requires all future implementations of that ISA to re-implement them, possibly to their detriment.

29. But perhaps the biggest challenge facing an ISA designer has to do with his or her motivation for attempting a new ISA design in the first place. There would have to be some very compelling reason why that designer believes it would be worth the enormous expense and risk of attempting to develop a custom ISA. That designer must therefore achieve the delicate balance required of any ISA while also maintaining the compelling innovation aspect of the new ISA, along with development of the

software tools (itself a gargantuan task), documentation, training, and creation and maintenance of validation suites. Another way to look at this is that, even if an existing ISA is not perfect for a particular implementation and therefore foregoes some potential performance or power savings, it is not a given that a new ISA could do so much better that performance alone could be a sufficient motivation for a new ISA development. In my career, I have had the opportunity to help develop a new ISA (at Bell Labs and Multiflow Computer), and as Intel's chief x86 architect, I oversaw the addition of hundreds of new instructions to x86 to keep the performance of x86 chips competitive. Indeed, the x86 ISA was considered doomed in the 1980s by most computer architecture researchers, who believed it was too archaic even then to remain competitive. Forty years later, with continuous development, it is still one of the most popular and profitable ISA for servers, desktops, and laptops.

30. Most system architects choose to license existing ISAs for the CPU parts of their new product. Rather than waste time and incur project risk by developing a new ISA, they can invest their limited time and resources in optimizing other essential aspects of the system: cache design, placement, policies, sizes and speeds; memory size, controller features, and power/performance tradeoffs; system power management and power-efficient operating states; and hardware accelerators for important functions or emerging applications. When they finish and begin marketing their new

CPU, being able to stamp the Arm-compliant imprimatur can be extremely valuable, because it raises the confidence of a prospective CPU purchaser concerning the maturity of the design, the tools available (and quality thereof), what backup plans might be feasible, and much more.

31. While SoC technology has been around since the 1970s, continuing advances in chip implementation technology, combined with steadily increasing user expectations, have converged to make SoCs the technology of choice. An SoC is at the heart of every smartphone, Apple or otherwise. An SoC, as exemplified below,⁴ is a combination of IP blocks for specific functions, comprising such modules as one or more CPU cores, a graphics processor, DRAM interfaces, a power management unit, and various I/O standard interfaces, all on a single chip.

⁴ *NVIDIA and Qualcomm ARM Up Against Competitors*, BERKELEY DESIGN TECHNOLOGY, INC. (October 18, 2011), <https://www.bdti.com/InsideDSP/2011/10/20/NvidiaQualcomm> (last visited December 19, 2023).

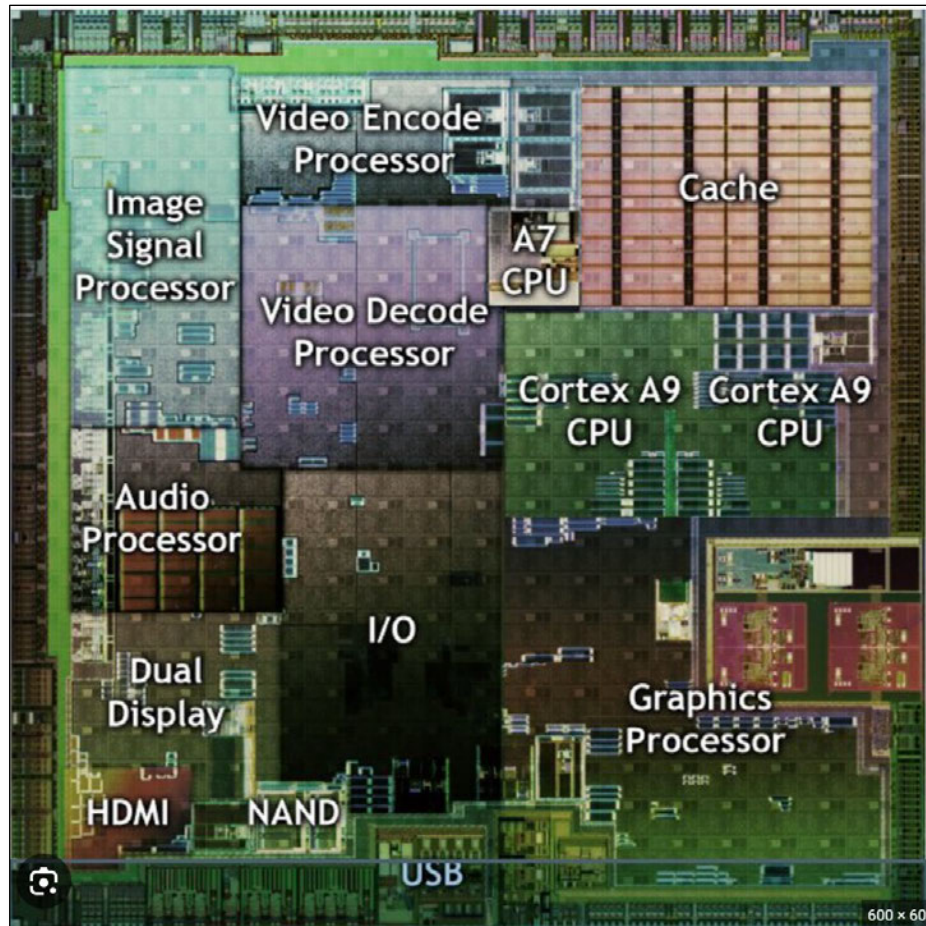


Figure 2: SoC showing various IP blocks and two CPU cores.

32. Systems with as many required features as modern SoCs rely heavily on industry standards to help manage that complexity. Today's SoCs have several different radio transmitter/receivers, and each of them corresponds to an industry standard, so that the final SoC will allow the user to successfully contact the cell phone tower, the local WiFi network(s), and a Bluetooth device attempting to pair with it. Similarly, there are industry standards for touchscreens, USB cables, batteries, chargers, and many other aspects of an SoC-based product. From a product designer's point of view, being compatible with communications standards is absolutely required:

buyers of their product will expect their new smartphone to reliably talk to cell phone towers using the appropriate cell phone radio protocols, send and receive data (and device charging current) via a USB cable, connect to nearby printers and headphones via Bluetooth, and so on.

33. One of the other choices the SoC designer will make concerns the ISA of the general processor (or processors, in the case of multiple cores) on the SoC. They will choose one of three options: (1) adopt an existing ISA such as Arm's ISA; (2) start with a "blank sheet" and design their own ISA (the "full custom" option); or (3) start with an existing ISA and modify it. The full custom option (2) is much more expensive than the other two, both in design and software tools support, and is risky. The first option is the most expedient and has a great deal to recommend it – for a reasonable licensing fee, the designer can license a known-working core (such as an Arm-designed core) that is compatible with the desired ISA, along with the software tool chain required to use it. There is broad industry acceptance of (1), as numerous companies license cores from Arm, including Nuvia, which had a TLA agreement. Some customers may want to add some feature or instruction to an existing ISA (option (3)), which retains the advantages of option (1) at a small cost in new software tool development, potentially resulting in a valuable product differentiation opportunity, but at the cost of additional development and permanent maintenance overhead.

34. The CPU is often described as the “brains” of a system. It executes a program that allows it to control the SoC: it oversees management of the battery subsystem, it runs whatever application(s) the user has indicated, it controls the display and reads the touchscreen inputs, and so on. CPUs work by “fetching” or retrieving an instruction from memory, decoding that instruction, performing the indicated operation, and then deciding what instruction is to be done next (which is usually the next sequential instruction in memory).

35. The CPU is designed to correctly perform all instructions from an “instruction set” using various machine resources such as registers (fast temporary storage), control/configuration registers, operating system facilities such as translation lookaside buffers, main memory, and input/output (I/O). CPUs must also strictly follow the ISA’s design for how to handle faults (such as divide-by-zero errors) and illegal instructions.

36. An instruction set is a collection of instructions that the CPU can perform, along with whatever information an assembly language programmer would need. Aside from the list of valid instructions, an assembly language programmer would need to know how many registers there are and whether any of them have side effects. They would also have to know how the ISA handles “memory semantics” (special rules one must follow to successfully interact with main memory), supported data types (such as integer, floating point, and strings), and the maximum size of virtual

and physical addresses. If a designer is developing a custom CPU core that is compliant with a particular ISA, the CPU design will need to comply with the constraints and requirements of that ISA.

37. CPUs can only perform instructions from the set of instructions for which they were designed. An Arm-compliant CPU cannot execute code for an x86, nor can an x86 processor execute Arm code. Both Arm and x86 have their own lists of instructions, Arm's list being shorter than x86's, each instruction encoded in its own way. If a processor fetches an instruction, and upon trying to decode that instruction discovers that the fetched bit pattern does not correspond to any of the instructions it understands, then the processor will perform a special maneuver called an "illegal instruction trap" and will terminate the application in which the illegal instruction appeared. Due to these issues of compatibility, it is imperative for designers to adopt an ISA that is broadly used, like the Arm ISA.

38. A microprocessor's ISA is often referred to by the shorthand "architecture"; *e.g.*, one might speak of the Intel Architecture or Arm Architecture. It is important to realize that any given architecture can be implemented in any number of different ways, each of them delivering different combinations of performance, power, cost, and size, while remaining compliant with the ISA.

3. Microprocessor Development.

39. A CPU architecture can be viewed as an abstract set of rules describing the interface between hardware and software – the interface as

seen by an assembly-language programmer. A CPU *microarchitecture*, by contrast, is the set of hardware functional blocks and protocols between those blocks that jointly implement the CPU architecture. A given CPU architecture may be implemented in a microarchitecture that optimizes performance above all else, including at the expense of high power and high product cost which would make it suitable for supercomputers and high-end servers. Conversely, that same CPU architecture can be realized via a different microarchitecture optimized for low power and long battery life, as required by mobile platforms such as tablets, smartphones, and laptops.

40. A CPU microarchitecture is implemented in a specialized low-level programming language called register transfer language (RTL). Examples of RTL include Verilog and VHDL. During development of a CPU core, a computer engineer uses a computer workstation to write and edit the RTL, adding new features or fixing errors. Then her work would be combined with that of her co-designers to constitute the current design. After innumerable such edit/fix/add/test sessions, the aggregate design will have implemented all necessary functionality to be considered compliant with the intended ISA. Automated software tools then translate the RTL into circuits and interconnections on the actual silicon substrate.

41. While the designers are modifying their RTL to complete the design and remove errors, a validation team is testing that RTL against legacy tests, random tests, and test suites. Design errors caught during RTL

development are generally orders of magnitude less expensive to ameliorate than “bugs” that escape into product deployment. It is easy to overlook the crucial role that validation plays in a processor development. As one CAD vendor put it: “In the field of electronics . . . verifying a design is universally the most critical aspect of a project. This applies to microprocessor design as well. Microprocessor designers generally require more time to verify their design than all other [design] steps combined.”⁵

42. It is not possible to test every bit pattern against every instruction against every possible exception condition – there are far too many combinations to try them all, even on the fastest computers. Instead, validation engineers use their intuition and experience to wield validation test suites, random testing, bespoke software tests, emulation systems, and large server farms, to help decide when a design has matured to the point where production can be considered. When the design team has finished RTL coding, and validation and management give the go-ahead, production commences.

43. Production consists of transferring the RTL database, through a set of electronic design automation tools, to a fabrication plant such as TSMC. There, the fab engineers will run the incoming RTL design through their own set of rigorous checks, looking for silicon design rule errors that

⁵ *The Microprocessor Chip: Design Guidelines, Functionality, and Characteristics*, CADENCE PCB SOLUTIONS (2020), <https://resources.pcb.cadence.com/blog/2020-the-microprocessor-chip-design-guidelines-functionality-and-characteristics> (last visited December 19, 2023).

would impact yield (such as on-chip wires that are too close together or inadequate power/ground planes). When the fab engineers are satisfied, the actual photochemical processing of making a silicon chip begins.

44. Silicon processing is performed on wafers, thin disks that can hold dozens or hundreds of individual chips. After many steps and having traversed many large photochemical “tools” within the fab, the wafer processing eventually completes. The fab then performs quick tests on each die on the wafer and marks any die that fails so that further effort will not be wasted on it. The remaining dice are cut from the wafer and tested further. Those that survive will be packaged for sale to customers.

4. Business Models for Licensing Microprocessor Architectures

45. As outlined above, SoC designers have several fundamental options to consider, including which ISA their CPUs will be compliant with. There are only a few available ISA choices: Arm, RISC-V, and potentially (in the future) x86.

46. Arm is the gold standard for licensing ISAs and ISA-compliant cores. It has been in the ISA business for 33 years and has successfully developed multiple versions of its ISA (the latest is version 9) and numerous Arm ISA-compliant cores. Where RISC-V is open-source, meaning all intellectual property within the ISA and tools are publicly available and royalty-free, Arm is closed-source: buy the license and use the tools, but be subject to Arm’s license requirements. In exchange, the licensee gets

consultation, documentation, guidance, and a relatively low-risk development path.

47. There are other advantages to an Arm license. The first is the intangible benefit of partnering with a company that has helped many others develop a successful product in the high-tech marketplace, and therefore is in a good position to evaluate a licensee's plans for new features and technical risks. A second is Arm's comprehensive portfolio of available technologies for other aspects of the licensee's product, such as on-chip interconnects that work well with the Arm ISA, and extensive validation suites that not only check architectural compliance but also serve as a thorough check on basic correctness of a new CPU implementation. Indeed, when Arm judges a new processor to be Arm-compliant, it is not just the processor designer's reputation at stake, it is also Arm's own reputation, which is a valuable endorsement for a chip design company, especially one with no previous track record.

48. RISC-V is a new ISA contender that is currently emerging with one major selling point – it is free. As one designer put it, “[i]f you wanted to make a CPU and you're not AMD or Intel, there are two real choices: ARM and RISC-V.”⁶

⁶ Matthew Connatser, *ARM vs. RISC-V: Is one better than the other?* DIGITALTRENDS (May 31, 2022), <https://www.digitaltrends.com/computing/arm-vs-risc-v/> (last visited December 15, 2023).

49. RISC-V was designed from the start to be “open source” – freely available and usable now and in the future. Support for the RISC-V open-source ISA may carry challenges. When a bug is found in a core design or in a critical software tool, who fixes it, and on what schedule? If a required feature is currently missing from a tool, who will develop that feature and maintain it, and when? If support is needed by a designer who has questions, who provides reliable answers on an urgent basis? Are future-looking ISA extensions being actively researched so that the RISC-V ISA will become and remain competitive in the future? RISC-V advocates argue that ISA customization will be increasingly important in a power-constrained future. Detractors point out that there is no guarantee that such innovations will be generally available, there being no requirement that RISC-V users share their advances. Both sides cite “fragmentation” where open-source users all run off in different directions with little central coordination (witness the wild proliferation of various Linuxes). RISC-V argues that it’s a good thing, allowing for innovation, while closed-source fans prefer standardization. All of this uncertainty adds up to considerable risk to a project development.

50. Qualcomm’s Manu Gulati (co-founder of Nuvia) stated that RISC-V is “in its very early stages” and “is not that mature today.” (Gulati Dep. Tr. 38:20-22, 39:4-7.) “Risk 5 is today where ARM ecosystem was, like, more than 10 years ago. So it is not ready for someone coming up with . . . a full-blown server product with all the software and the tool chains and OSes

and everything that we've been talking about for software. It is not ready for that." (*Id.* at 38:22-25, 39:1-4.)

51. Intel has announced that it will begin x86 core licensing soon, but for the past 30 years, it declined to make x86 available and guarded its ISA zealously, so whether reasonably priced x86 cores at competitive performance and availability will appear is currently unknown.

B. Parties

1. Arm

(i) Company Background

52. Arm was established in 1990 with the goal of developing computer processors that were highly power efficient. Prospectus⁷ at 3. By the mid-1990s, Arm-based processors had gained traction in mobile phones due particularly to the energy efficiency of the processors. (*Id.*)

53. Arm's success with mobile phones has grown substantially over the years. Arm's technology is now present in 99% of the world's smartphones. As of the beginning of 2023, Arm estimates that its technology is present in 250 billion processors worldwide and that approximately 70% of the world's population uses Arm-based products. (*Id.* at 11.)

54. Arm is a major technology company, with annual revenue of approximately \$2.6 billion and almost 6,000 full-time employees. (*Id.* at 12.)

⁷ Arm Holdings plc., 95,500,000 American Depositary Shares (Representing 95,500,000 Ordinary Shares) (Form SEC-424B4) (September 13, 2023), <https://www.sec.gov/Archives/edgar/data/1973239/000119312523235320/d550931d424b4.htm> (last visited December 15, 2023) (hereafter "Prospectus").

About 80% of Arm's employees are devoted to research and development (R&D) (*id.*), and the company spends approximately \$1.3 billion per year on R&D efforts (*id.* at 110). Arm has business relationships with some of the world's biggest technology companies, including Apple, Samsung, Amazon, Mercedes Benz, and Siemens AG. (*Id.* at 14.) Arm is an owner or co-owner of approximately 6,800 issued patents. (*Id.* at 20.)

(ii) Arm Architecture

55. Arm's R&D efforts include developing and improving the Arm architecture, which Arm licenses to customers who wish to develop their own Arm-compliant custom cores under an Architecture License Agreement (ALA). Arm also provides development tools to assist ALA customers with implementing the Arm architecture in custom Arm-compliant cores.⁸

56. The Arm architecture includes the set of instructions that an Arm-compliant processor must be able to execute. These Arm instructions form the basis of the ISA. In addition to the required instructions, the Arm ISA includes other information that is needed to execute the instructions, such as information about registers that store data, encoding of data, and supported data types. The Arm architecture further includes information about exception detection and handling addressing modes, memory access ordering, special register semantics, operating system support functions, control registers, rules for co-processors, context swap information,

⁸ ARM, <https://www.arm.com/products/development-tools> (last visited December 15, 2023).

interrupts, breakpoints, boot procedures, privileged modes, various abort vectors, security features, fencing and atomic operation support, and memory alignment restrictions. Arm has offered a number of versions of its ISA over the years, with the latest being version 9.⁹

57. The Arm architecture is described in documentation provided by Arm, specifically the Arm Architecture Reference Manual, sometimes called the “Arm ARM.” Arm also provides other documentation and technical support to its customers to help them develop processors that embody the Arm architecture and other Arm technology.

58. Based on my discussions with Arm Chief Architect Richard Grisenthwaite, the Arm ARM is the authoritative document that defines the Arm architecture. It is thousands of pages long and contains more information and detail than any engineering team could recall with precision. Thus, any engineering team designing a custom Arm-compliant core would need to regularly consult the Arm ARM and implement its contents in the RTL code design for the custom Arm-compliant core. Mr. Grisenthwaite noted that [REDACTED]

[REDACTED]. The Arm ARM contains a great many technical details concerning the Arm architecture that need to be correctly implemented in a core for it to be Arm-compliant.

⁹ ARM, *Arm CPU Architecture: A Foundation for Computing Everywhere*, <https://www.arm.com/architecture/cpu> (last visited December 15, 2023).

59. The types of information included in the Arm ARM includes the number, types, and any special aspects of the general register set; an introduction to the architecture and the instruction set; a discussion of the Programmer's Model (general information for an assembly language programmer, such as modes, exceptions, and synchronization primitives); details of the memory hierarchy design, including caches, write buffers, exceptions, and the like; architectural provisions for incorporating co-processors; features and design choices built into the virtual addressing mechanism; extensive discussions about the new floating point vector instructions and their use; and coverage of the built-in Debug Architecture.

60. While the Arm ARM is a publicly available document, I understand that the technology described in the Arm ARM is protected at least by patents and copyrights, as discussed below. Even though it is publicly available, the Arm ARM is still the subject of license restrictions with individual customers. For example, version G.b of the Arm ARM (ARM_01324149) includes the following restrictions:

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(ARM_01324149 at -150.)

Confidentiality Status

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(ARM_01324149 at -151.)

61. Arm updates the Arm ARM periodically as it continues to develop and improve upon the Arm architecture. Arm releases different versions of the Arm ARM to describe updated features. The second page of the document lists the various versions and identifies the changes from the prior version.

03 June 2016	A.j	Non-Confidential EAC	EAC release
30 September 2016	A.k	Non-Confidential Armv8.0 EAC	Updated EAC release
31 March 2017	B.a	Non-Confidential Armv8.1 EAC, v8.2 Beta	Initial release incorporating Armv8.1 and Armv8.2
26 September 2017	B.b	Non-Confidential Armv8.2 EAC	Initial Armv8.2 EAC release, incorporating SPE
20 December 2017	C.a	Non-Confidential Armv8.3 EAC	Initial Armv8.3 EAC release
31 October 2018	D.a	Non-Confidential Armv8.4 EAC	Initial Armv8.4 EAC release
29 April 2019	D.b	Non-Confidential Armv8.4 EAC	Updated Armv8.4 EAC release incorporating accessibility changes
05 July 2019	E.a	Non-Confidential Armv8.5 EAC	Initial Armv8.5 EAC release
20 February 2020	F.a	Non-Confidential Armv8.6 Beta	Initial Armv8.6 Beta release
31 March 2020	F.b	Non-Confidential Armv8.5 EAC, v8.6 Beta	Armv8.5 EAC release, initial Armv8.6 Beta release
17 July 2020	F.c	Non-Confidential Armv8.6 EAC	Initial Armv8.6 EAC release
22 January 2021	G.a	Non-Confidential Armv8.7 EAC	Initial Armv8.7 EAC release
22 July 2021	G.b	Non-Confidential Armv8.7 EAC	Updated Armv8.7 EAC release

(ARM_01324149 at -150.)

62. An ALA allows a customer to develop its own customized core that is compliant with the Arm architecture. Prospectus at 96. According to Mr. Grisenthwaite, [REDACTED]

[REDACTED]. [REDACTED]

[REDACTED]

[REDACTED]

63. I discussed with Mr. Grisenthwaite the types of support that Arm provides to its customers. He noted that [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

(iii) Arm Processors

64. Arm also offers its customers a variety of Arm-developed processor products, including its Cortex CPUs, GPUs, Physical IP, System IP, Security IP, and Subsystems IP.¹⁰ When a core is compatible with Arm, it can interoperate with other Arm-developed products. For example, the Nuvia/Qualcomm NCCs and SoCs included cores that interoperated with

¹⁰ ARM, <https://www.arm.com/products> (last visited December 15, 2023).

other IP blocks from Arm. Thus, there is an ecosystem of Arm IP and tools from which those designing their own Arm cores can benefit. A company can license the Arm processor products and IP blocks under a Technology License Agreement (“TLA”). Prospectus at 96. Under a TLA, customers are provided with “off-the-shelf” Arm CPUs and IP blocks that are compliant with the Arm architecture.

65. Arm’s Cortex CPUs include the Cortex-A, Cortex-R, and Cortex-M families. The Cortex-A processors are CPUs for general use with operating systems and third-party applications.¹¹ The Cortex-R processors are embedded processors for real-time digital signal processing and control.¹² The Cortex-M processors are microcontrollers.¹³

66. Arm’s processors are used for many different applications in different markets, including consumer technologies (*e.g.*, personal computers, smartphones, tablets),¹⁴ automotive,¹⁵ cloud computing,¹⁶ and Internet of Things (IoT).¹⁷

¹¹ ARM, <https://www.arm.com/product-filter?families=cortex-a&showall=true> (last visited December 15, 2023).

¹² ARM, <https://www.arm.com/products/silicon-ip-cpu?families=cortex-r> (last visited December 15, 2023).

¹³ ARM, <https://www.arm.com/products/silicon-ip-cpu?families=cortex-m&showall=true> (last visited December 15, 2023).

¹⁴ ARM, <https://www.arm.com/markets/consumer-technologies> (last visited December 15, 2023).

¹⁵ ARM, <https://www.arm.com/markets/automotive> (last visited December 15, 2023).

¹⁶ ARM, <https://www.arm.com/markets/computing-infrastructure> (last visited December 15, 2023).

¹⁷ ARM, <https://www.arm.com/markets/iot> (last visited December 15, 2023).

**(iv) Arm Has a Large Patent Portfolio
Covering Its Architectural
Innovations**

67. One of the ways Arm protects its proprietary technology is by seeking patent protection for its innovations. Prospectus at 148. As of March 31, 2023, Arm owns or co-owns approximately 6,800 issued patents and has approximately 2,700 pending patent applications worldwide. (*Id.*) The patents cover aspects of Arm's processor architecture and microarchitecture, including certain specific instructions. (*Id.*) By patenting its technology, Arm retains IP rights in the Arm architecture that it licenses to its customers, even while making the Arm ARM available to the public.

68. I spoke with Mr. Grisenthwaite regarding Arm's patent portfolio. He confirmed that [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]¹⁸

**(v) Industry Adoption of Arm
Architectures**

69. Arm-based CPUs are the most popular and pervasive CPUs in history. Prospectus at 12. As I mentioned above, ARM-based CPUs are in 99% of the world's smartphones and Arm estimates that 70% of the world's population uses Arm-based products. Prospectus at 11. More than

¹⁸ By way of example, Mr. Grisenthwaite identified [REDACTED].

260 companies report that they shipped Arm-based chips in the fiscal year ending on March 31, 2023, including the world's largest companies like Amazon, Google, AMD, Intel, MediaTek, NVIDIA, and Samsung. (*Id.*) The Arm architecture and Arm-based CPUs have been adopted throughout the industry.

2. Qualcomm

70. Qualcomm is a technology company whose primary focus is on developing and commercializing technology for mobile devices and other wireless products.¹⁹ Qualcomm principally derives revenue from sales of its integrated circuit products, including its Snapdragon family of products, and licensing of its intellectual property. Qualcomm Annual Report at 8. Around 2017, Qualcomm sought to develop a custom Arm-based CPU for data centers. Qualcomm called the custom core “Falkor” and the related SoC “Centriq.”²⁰ This effort was not ongoing at the time of the Nuvia acquisition, since the president of Qualcomm’s data center business unit had left and the media reported that Qualcomm planned to offload the division.²¹ [REDACTED]

¹⁹ Qualcomm, Annual Report (Form 10-K) (September 26, 2021), <https://www.sec.gov/Archives/edgar/data/804328/000172894921000076/qcom-20210926.htm> (last visited December 15, 2023) (hereafter Qualcomm Annual Report).

²⁰ *Introducing the Qualcomm Falkor CPU core: purpose-built for cloud workloads*, QUALCOMM, OnQ Blog (August 19, 2017), <https://www.qualcomm.com/news/onq/2017/08/introducing-qualcomm-falkor-cpu-core-purpose-built-cloud-workloads> (last visited December 15, 2023).

²¹ James Morra, *With Future Uncertain, Qualcomm Loses Data Center President*, ELECTRICDESIGN (May 22, 2018), <https://www.electronicdesign.com/markets/automation/article/21806539/with-future-uncertain-qualcomm-loses-data-center-president> (last visited December 15, 2023).

[REDACTED]

[REDACTED]

[REDACTED]

QCARM_3520804.)

3. Nuvia

a. Company Background

71. Nuvia was founded as a start-up in 2019 by ex-Apple engineers Gerard Williams III, Manu Gulati, and John Bruno.²² Mr. Williams was previously an ARM fellow at Arm for twelve years ([REDACTED]) and was also the Chief Architect at Apple for the M1 processor, which was a custom Arm-compliant CPU for consumer devices like laptops. ([REDACTED] [REDACTED] [REDACTED]) Nuvia planned to design energy-efficient

²² Danny Crichton, *Three of Apple and Google's former star chip designers launch NUVIA with \$53M in series A funding*, TECHCRUNCH (November 15, 2019), <https://techcrunch.com/2019/11/15/three-of-apple-and-googles-former-star-chip-designers-launch-nuvia-with-53m-in-series-a-funding/> (last visited December 15, 2023).

CPUs for data center servers based on the Arm architecture.²³ At the time, designing a processor for data centers would have expanded the market for Arm's technology, since the data center market was historically dominated by x86 architectures. () Nuvia named its custom Arm-based CPU core " ()

b. Nuvia's ALA and TLA

(i) Background of Nuvia's ALA and TLA

72. On September 26, 2019, Arm and Nuvia entered into both an ALA (ARM_00059183) and a TLA (ARM_00002988). On September 27, 2019, Arm and Nuvia entered into an Annex 1 for both the ALA (QCARM_0339310) and the TLA (ARM_00051126). On March 27, 2020, Arm and Nuvia entered into another Annex 1 for both the ALA (ARM_00057230) and the TLA (QCARM_3861394).

73. As I explained in § III.B.1.ii, above, ALAs generally provide the licensee with the right to develop and produce a custom core that is compliant with the Arm architecture.

74. I am not an expert on licensing, but I have reviewed the Nuvia ALA agreement (including both Annex 1 documents). As I understand it, the Arm-Nuvia ALA agreement gave Nuvia the right to design and market a custom Arm-compliant core under that agreement. The Arm-Nuvia ALA

²³ Dean Takahashi, *Nuvia raises \$240 million to design Arm-based CPUs for datacenters*, VENTUREBEAT (September 24, 2020), <https://venturebeat.com/business/nuvia-raises-240-million-to-design-arm-based-cpus-for-datacenters/> (last visited December 15, 2023).

agreement provided Nuvia with access to [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED].

(ii) Definition of [REDACTED]

75.

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

76.

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

(ARM_00057230 at -231.)

77. According to my understanding from reviewing the documents,

[REDACTED]

As Mr. Grisenthwaite explained in his deposition, the ALA [REDACTED]

[REDACTED]

78. [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

79. [REDACTED]

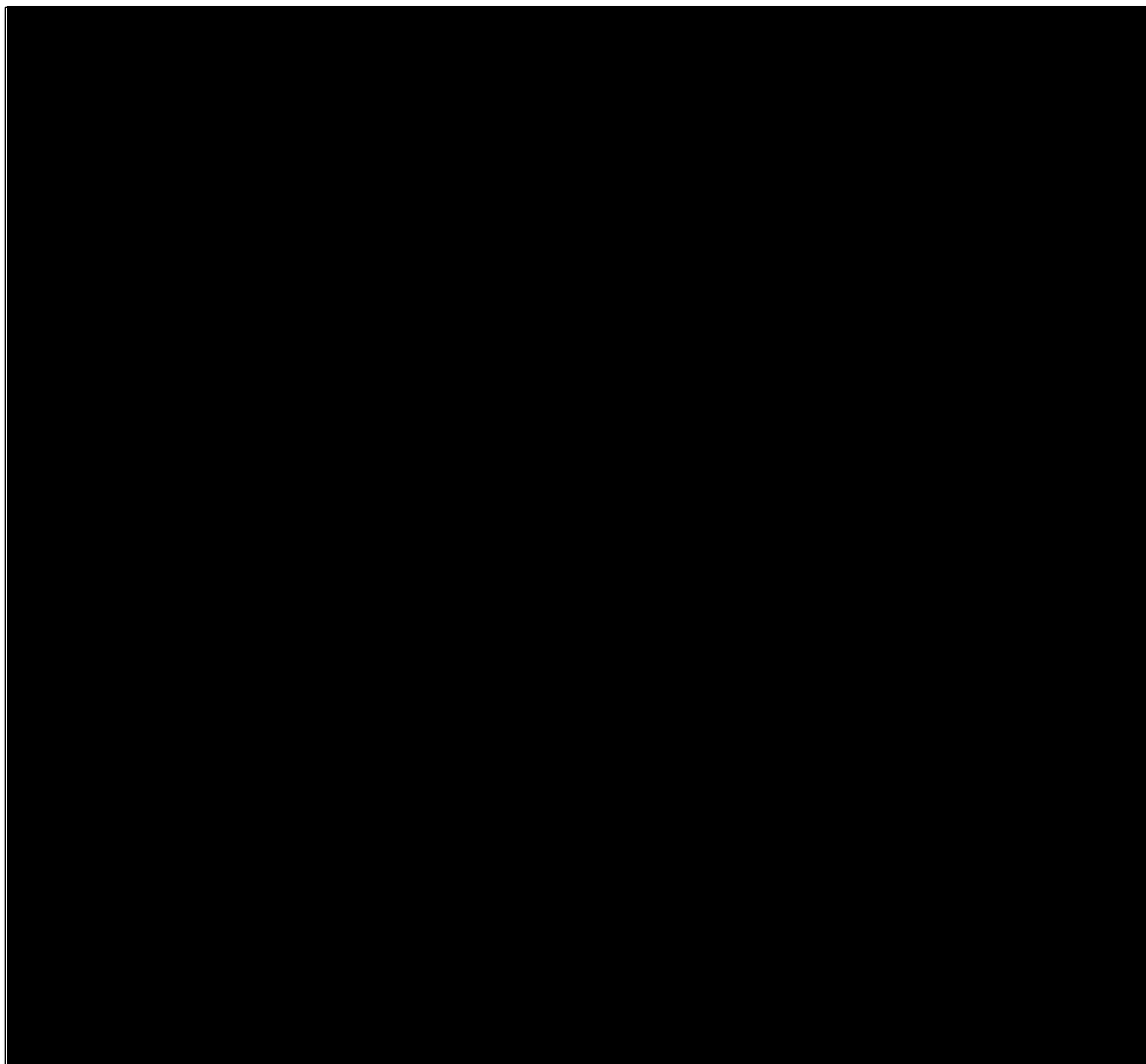
[REDACTED]

[REDACTED]

(ARM_00057230 at -231.)

80. The “ARMv8-A Architecture Compliance Kit” (ACK), product code [REDACTED] includes, among other things, [REDACTED]

[REDACTED]



(ARM_00057230 at -231-232.)

81.

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]. Arm's Richard Grisenthwaite told me [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

(ARM_00057230 at -232.)

83. Computer security has become an essential element of modern systems, particularly systems through which valuable information flows (such as credit card numbers or bank account data). These systems, including smartphones, are actively and routinely attacked, so in response, these information flows must be encrypted by the sender and decrypted by the receiver. Encryption and decryption algorithms are computationally quite intensive, yet must be performed quickly enough that system users do not become impatient. [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

(iii)

[REDACTED]

84.

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

85. At every step of CPU development, hundreds of decisions are made that balance the various project goals against the fixed requirements of the ISA. Nearly every aspect of the RTL implicitly reflects the influences of the [REDACTED] – [REDACTED]

[REDACTED] Arm

also provides [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

86. My understanding is consistent with that of Mr. Grisenthwaite, who told me that [REDACTED]

[REDACTED]

[REDACTED]

Similarly, I consider [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

87. Likewise, if a licensee has chosen to implement [REDACTED] [REDACTED], obviously the instruction decoder design will necessarily reflect that, since it has to detect and decode all CPU instructions. Beyond that, however, inclusion of [REDACTED] will impact the microarchitecture in several distinct ways that are unique to Arm-compliant CPUs: a [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

²⁴ As I mentioned in § III.B.3.b.iv below, the termination provision of the Nuvia ALA states:

[REDACTED]

(iv) Termination Provision

88. From my review of the documents, it is my understanding that [REDACTED] of the Nuvia ALA discusses Nuvia's obligations if Arm terminates the ALA. (ARM_00059183 at -196.) This section references the [REDACTED] [REDACTED] definition, which I previously discussed:

[REDACTED]

(Id.)

89. From my review, I understand that [REDACTED] requires that upon termination of the ALA by Arm, Nuvia is required to [REDACTED]

[REDACTED]
[REDACTED]
[REDACTED]
[REDACTED]
[REDACTED] As I

explained in § III.B.3.b.iii, above, my understanding as a technical and

industry expert is that [REDACTED] include [REDACTED]
[REDACTED]
[REDACTED]

C. Factual Background

1. Nuvia Develops the [REDACTED] in Compliance with the Arm Architecture

90. Nuvia developed an SoC codenamed “[REDACTED]” that was designed for the data center market. (QCARM_2402257 at -263.) [REDACTED] included a custom CPU core called “[REDACTED] ([REDACTED])”
[REDACTED]
[REDACTED]

[REDACTED]

(QCARM_2402257 at -269.)

[REDACTED]

(QCARM_2402257 at -270.)

[REDACTED]

(QCARM_2402257 at -318.)

91. Nuvia designed the [REDACTED] core in accordance with the Armv8-A architecture described in the Arm ARM. [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED] (*See*

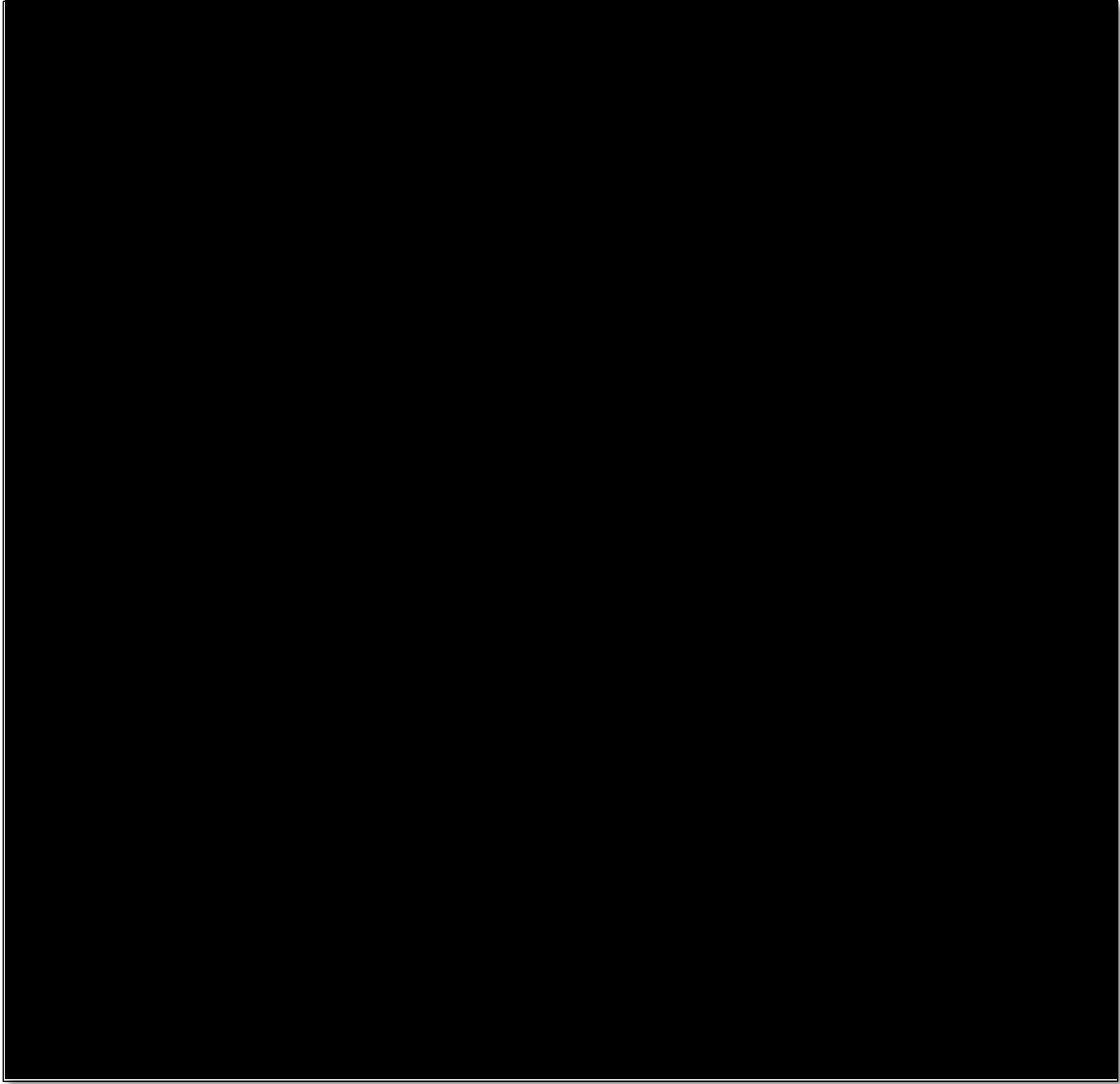
QCARM_3087757, QCARM_3087992, QCARM_0325086, QCARM_0490031, QCARM_3088245, QCARM_3089361, QCARM_3087396, QCARM_3088553, QCARM_0325371, QCARM_0490329, QCARM_3088937.)

92. [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]



(QCARM_3087757 (highlighting added).)

93. [REDACTED]
- [REDACTED]
- [REDACTED]
- [REDACTED]
- [REDACTED]
- [REDACTED]
- [REDACTED]
- [REDACTED]

94.

95.

2. Qualcomm Purchases Nuvia and Arm Objects

96. As I explained in § III.B.1.i, above, Arm established dominance in the mobile processor market in the 1990s and Arm remains recognized as the premier CPU provider for the mobile processor market.²⁵ Arm technology was in 90% of smartphones as far back as 2010, and its market share of the

²⁵ William Gayde, *How Arm Came to Dominate the Mobile Market*, TECHSPOT (December 24, 2020), <https://www.techspot.com/article/1989-arm-inside/> (last visited December 15, 2023).

mobile processor market has only grown since then, with Arm “dominat[ing] the mobile processor market with almost every major release built on top of its architecture.” (*Id.*)

97. Arm licensee Apple launched its M1 SoC on November 10, 2020,²⁶ designed for personal computers. The M1 SoC uses a custom Arm processor as opposed to an x86 processor from Intel.²⁷ The M1 was an instant hit, as it was touted as being more efficient, operating faster, and having a longer battery life than competing SoCs, all with the use of a custom Arm processor. (*Id.*)

98. The release of the M1 SoC catapulted Arm into the PC market, as the M1 SoC was quickly recognized as outperforming other SoCs on the market.²⁸ The Apple M1 has since been viewed as a game changer in the CPU processor world and has helped Apple capture over 21% of the global PC

²⁶ APPLE, Press Release: Apple unleashes M1 (November 10, 2020), <https://www.apple.com/newsroom/2020/11/apple-unleashes-m1/> (last visited December 15, 2023).

²⁷ Nermin Hajdarbegović, *Apple M1 Processor Overview and Compatibility*, TOPTAL, <https://www.toptal.com/apple/apple-m1-processor-compatibility-overview> (last visited December 15, 2023).

²⁸ Stephen Shankland, *Apple M1 Macs are kick-starting a new Arm-based PC era. Arm's CEO is optimistic*, CNET (January 13, 2021), <https://www.cnet.com/tech/computing/apple-m1-macs-are-kick-starting-new-arm-based-pc-era-arm-ceo-is-optimistic/> (last visited December 15, 2023).

market.²⁹ With the expansion into the PC market, Arm is now recognized as a major player in designing CPU chips used in PCs.³⁰

99. Following the rise of Apple's M1 chip, Qualcomm considered purchasing Nuvia, which was developing its own Arm-based custom CPU core. [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

(QCARM_3536689.)

²⁹ Urvish Mahajan, *Apple M1 — How Apple Silicon Changed the PC Industry*, MEDIUM (September 23, 2023), <https://medium.com/@urvishmahajan/apple-m1-how-apple-changed-the-pc-industry-4a7c3c8a3d57#:~:text=The%20M1%20chip%20powered%20MacBook,Window's%20growth%20was%20just%206%25> (last visited December 15, 2023).

³⁰ Katie Tarasov, *How Arm is gaining chip dominance with its architecture in Apple, Nvidia, AMD, Amazon, Qualcomm and more*, CNBC (November 9, 2023), <https://www.cnbc.com/2023/11/09/how-arm-gained-chip-dominance-with-apple-nvidia-amazon-and-qualcomm.html> (last visited December 15, 2023).

100.

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

(QCARM_3536628.)

101.

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

102. On January 13, 2021, Qualcomm announced that Qualcomm Technologies, Inc. was acquiring Nuvia for \$1.4 billion. (QCARM_2423540.)

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

103. [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

104.

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

105.

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

106.

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED] Qualcomm has represented to the media that “the creation of our custom CPU was started by Nuvia engineers while employed at Nuvia.”³¹

107. On March 1, 2022, the Nuvia licenses terminated, along with the corresponding rights to use or sell products based on or incorporating Nuvia technology developed under those licenses. (QCARM_0338883.)

108. [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

3. Qualcomm Incorporates Nuvia Cores Into Its Own Products

109. After acquiring Nuvia, Qualcomm incorporated Nuvia's work on the [REDACTED] core into Qualcomm's own products. [REDACTED]

[REDACTED]

[REDACTED]

³¹ Mark Hachman, *Qualcomm dubs Nuvia CPU 'Oryon,' on track for 2023*, PCWORLD (November 17, 2022), <https://www.pcwORLD.com/article/1382740/qualcomm-dubs-nuvia-cpu-oryon-on-track-for-2023.html> (last visited December 16, 2023).

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED] I would expect that Qualcomm used Nuvia’s pre-acquisition work on the [REDACTED] core to further develop the [REDACTED] core that was submitted to Arm for verification. Consistent with my expectations, Qualcomm representatives have been quoted in the press as saying that “the creation of our custom CPU was started by Nuvia engineers while employed at Nuvia.”³² Also, as described below, Dr. Chen’s analysis of the RTL code for the [REDACTED] cores establishes that a significant portion of the [REDACTED] RTL code developed at Nuvia was incorporated into the later versions of the [REDACTED] core developed by Qualcomm.

110. [REDACTED]

[REDACTED]

[REDACTED]

³² Mark Hachman, *Qualcomm dubs Nuvia CPU ‘Oryon,’ on track for 2023*, PCWORLD (November 17, 2022), <https://www.peworld.com/article/1382740/qualcomm-dubs-nuvia-cpu-oryon-on-track-for-2023.html> (last visited December 16, 2023).

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

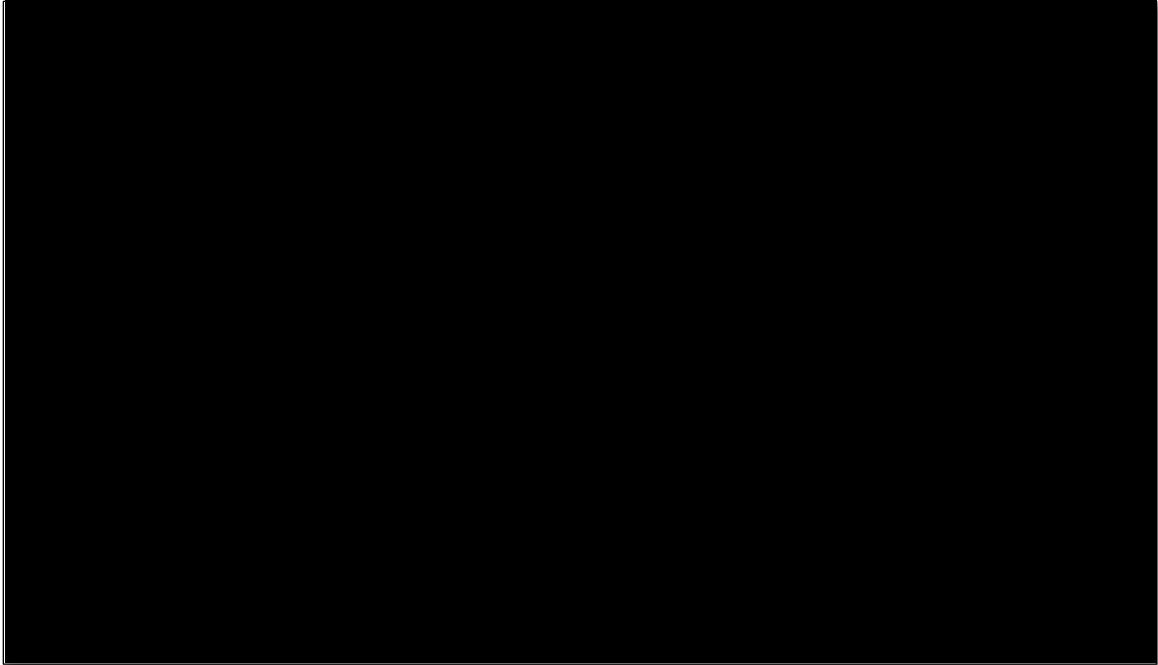
111. [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]



(QCARM_0181949 at -950.)

112.

[Redacted]

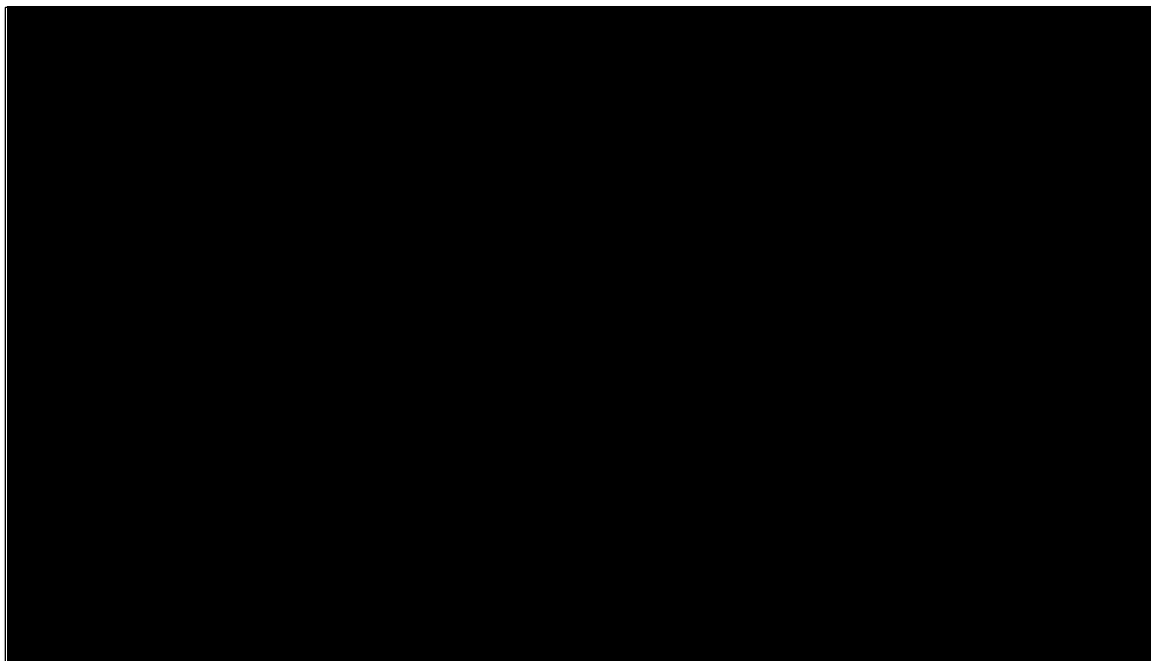
[Redacted]

[Redacted]

[Redacted]

[Redacted]

[Redacted]



(QCARM_0182011 at -019.)

113.

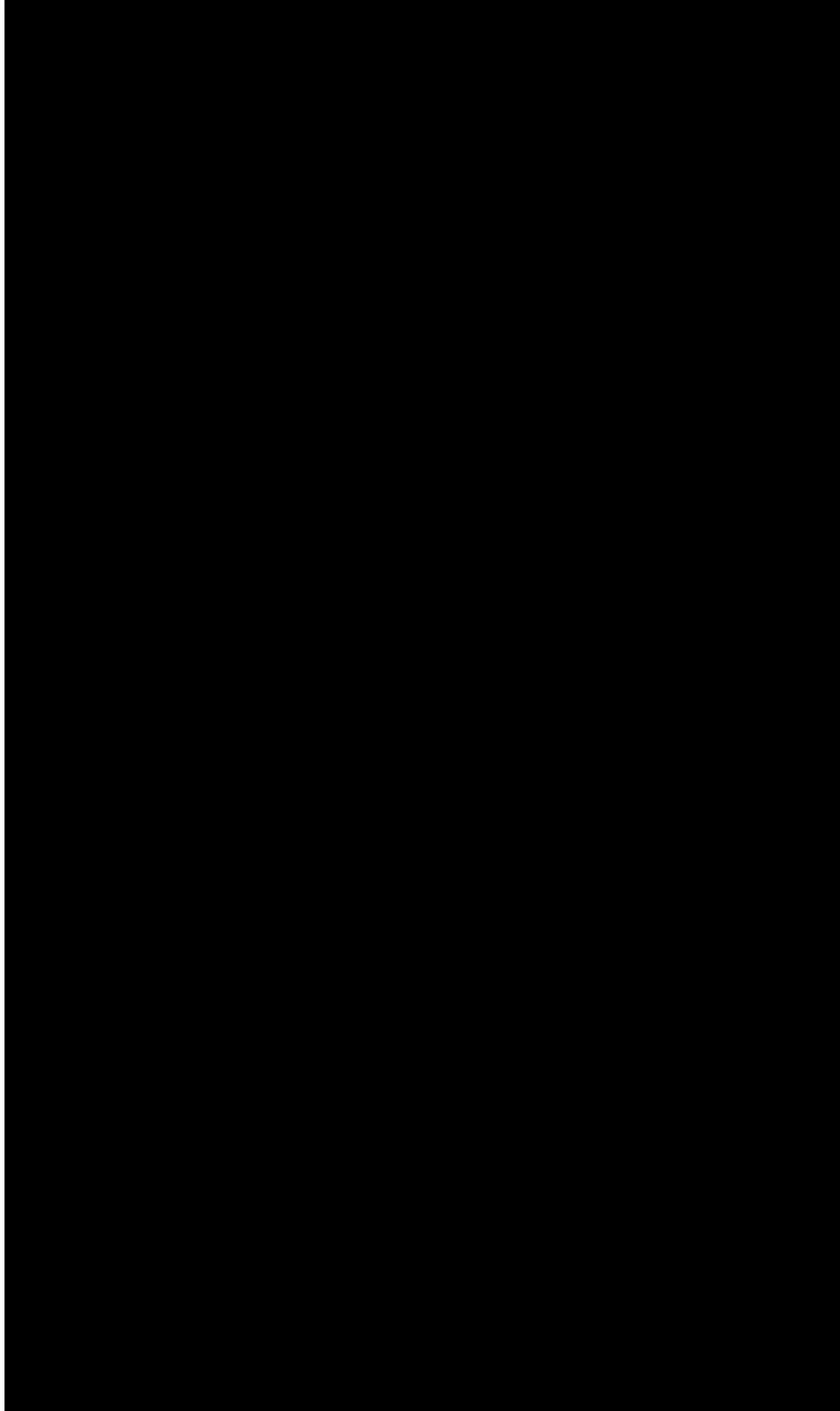
[REDACTED]

[REDACTED]

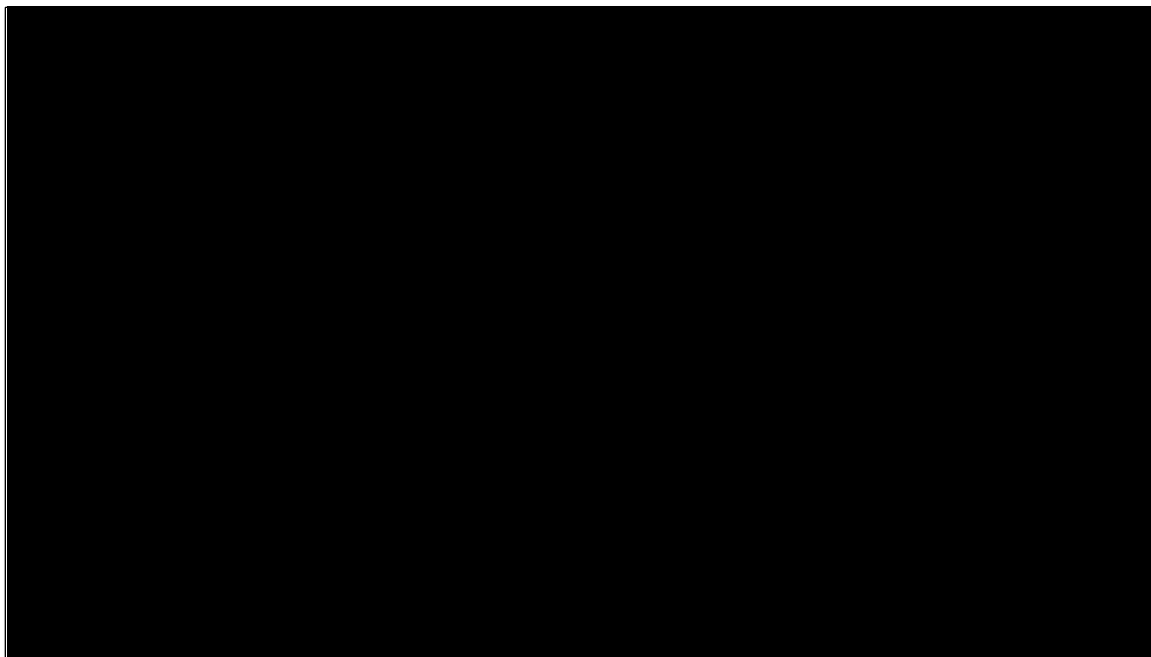
[REDACTED]

[REDACTED]

[REDACTED]

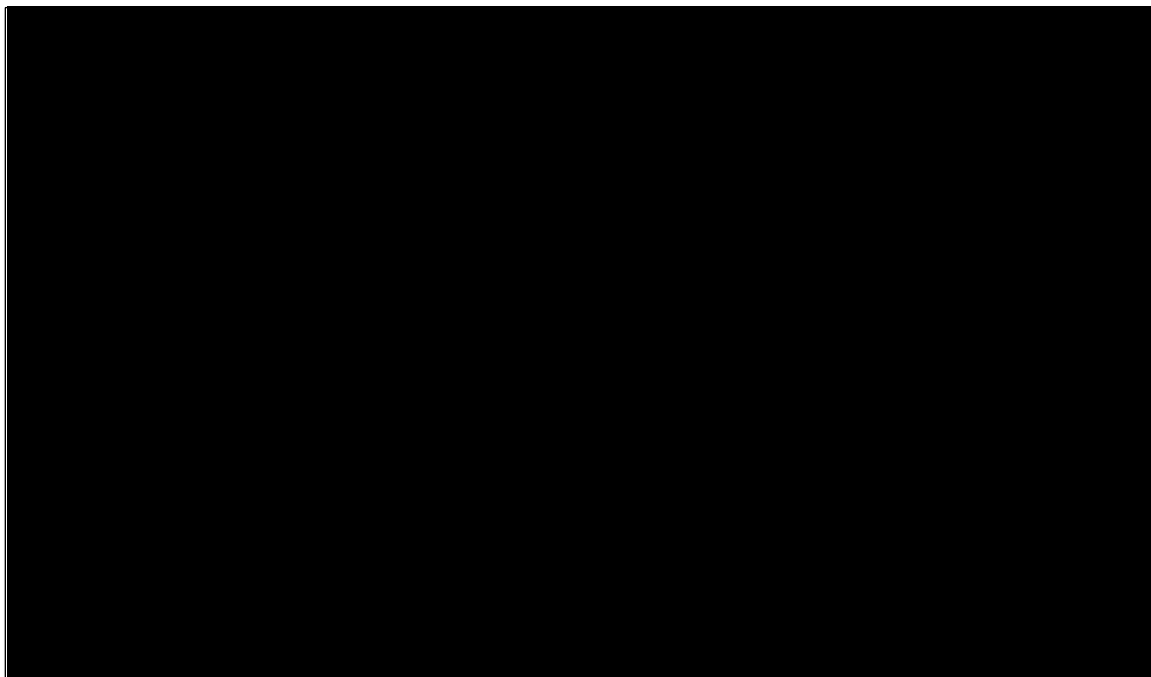


(QCARM_0169739 at -744 (cropped for visibility).)



(QCARM_0169739 at -749.)

114.



(QCARM_0550518 at -521.)

4. Qualcomm Releases Snapdragon X

115. On October 24, 2023, Qualcomm announced its new Snapdragon® X Elite platform of SoCs, with what it called its “custom integrated Qualcomm Oryon CPU.”³³ Qualcomm’s attorneys represented that they produced source code corresponding to Oryon: “Oryon is a brand name and does not refer to a specific project or piece of technology. Qualcomm has produced source code for the custom CPUs that will be sold under the Oryon name.” (10/26/2023 email from J. Braly to J. Li.) Based on these representations and the dates of the produced source code (*see* § IV.B, below), it is my understanding that the October 24, 2023 [REDACTED] [REDACTED] code corresponds to the Qualcomm Oryon CPU announced on the same date, making the Snapdragon® X Elite platform of SoCs and Qualcomm Oryon CPU [REDACTED] [REDACTED]

5. Abbreviated Timeline of Events

116. Below is an abridged timeline of events for this case.

Date	Event
Feb. 2019	Gerard Williams III, John Bruno, and Manu Gulati found Nuvia. ³⁴

³³ QUALCOMM, Press Note: Qualcomm Unleashes Snapdragon X Elite: The AI Super-Charged Platform to Revolutionize the PC (Oct. 24, 2023), <https://www.qualcomm.com/news/releases/2023/10/qualcomm-unleashes-snapdragon-x-elite--the-ai-super-charged-plat> (last visited December 16, 2023).

³⁴ Dean Takahashi, *Nuvia raises \$240 million to design Arm-based CPUs for datacenters*, VENTUREBEAT (Sept. 24, 2020), <https://venturebeat.com/business/nuvia-raises-240-million-to-design-arm-based-cpus-for-datacenters/> (last visited December 15, 2023).

Sep. 27, 2019	Arm and Nuvia enter into the Architecture License Agreement (ALA) and the Technology License Agreement (TLA). ³⁵
Aug. 11, 2020	Nuvia announces the [REDACTED] core. ³⁶
Mar. 16, 2021	Qualcomm completes acquisition of Nuvia. ³⁷
Feb. 1, 2022	Arm notifies Nuvia that it intends to terminate the ALA and the TLA due to Nuvia's violation of the assignment provisions. The termination is to be effective as of Mar. 1, 2022. ³⁸
[REDACTED]	[REDACTED]
Mar. 1, 2022	Effective date of termination of Nuvia ALA and TLA. ⁴⁰
[REDACTED]	[REDACTED]
[REDACTED]	[REDACTED]
Aug. 31, 2022	Arm files a complaint against Qualcomm and Nuvia for breach of contract and trademark infringement in the U.S. District Court for the District of Delaware. ⁴³

³⁵ (QCARM_0337839; QCARM_0338297.)

³⁶ Matthew Connaster, *Nuvia Announces CPI Codenamed [REDACTED] Promises to Deliver Leading Single Threaded Performance*, ADORED TV (August 11, 2020), [https://adoredtv.com/nuvia-announces-cpu-codenamed-\[REDACTED\]-promises-to-deliver-leading-single-threaded-performance/](https://adoredtv.com/nuvia-announces-cpu-codenamed-[REDACTED]-promises-to-deliver-leading-single-threaded-performance/) (last visited December 20, 2023).

³⁷ (QCARM_2402586.)

³⁸ (QCARM_0338883.)

³⁹ (QCARM_0557206.)

⁴⁰ (QCARM_0338883.)

⁴¹ (QCARM_3433989.)

⁴² (QCARM_0190735.)

⁴³ (ARM_00045395.)

IV. FURTHER OPINIONS⁴⁴

A. The [REDACTED] Cores Were Designed as [REDACTED]
[REDACTED] and Are [REDACTED]

1. Relevant Technical Definitions from Nuvia
ALA and Annex.

117. [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

118. [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

119. [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

⁴⁴ In addition to my opinions set forth in § IV, I note that I have provided some opinions in the Background (§ III). I incorporate any opinions from the Background (§ III) into the Opinion (§ IV).

120.

[REDACTED]

121.

[REDACTED]

[REDACTED]

[REDACTED]

(*Id.*)

122.

[REDACTED]

[REDACTED]

123.

[REDACTED]

[REDACTED]

2. The Nuvia [REDACTED] Core and Later Versions of the [REDACTED] Core Were Designed to Implement the Elements of the Armv8 Architecture.

a. Nuvia decided to create a custom core based on the Arm architecture.

124. Since its founding, Nuvia's vision was to create an enterprise-level data server processor using the Armv8 architecture.

(QCARM_3314892 at -893, -905.) [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

125. [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

b.

[REDACTED]

(i)

126.

<p> <input type="checkbox"/> Yes <input type="checkbox"/> No <input type="checkbox"/> Don't know </p>	<p> <input type="checkbox"/> Yes <input type="checkbox"/> No <input type="checkbox"/> Don't know </p>
--	--

(ii)

[REDACTED]

127.

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

(*Id.* at -772-773.)

128. [REDACTED]

[REDACTED]

129. [REDACTED]

[REDACTED]

[REDACTED]	Phoenix Cores ⁴⁶
[REDACTED]	[REDACTED]
[REDACTED]	[REDACTED]
[REDACTED]	[REDACTED]
	[REDACTED] ⁴⁹

⁴⁵ Requirements listed in Nuvia Annex [REDACTED]

⁴⁶ [REDACTED]

⁴⁷ *Id.* at -772.

⁴⁸ *Id.* at -972.

⁴⁹ *Id.* at -772.

[illegible]

130.

⁵⁰ *Id.* at -813.

⁵¹ *Id.* at -922.

⁵² *Id.* at -773.

⁵³ “The Armv8 A-profile architecture includes a *Virtual Memory System Architecture* (VMSA).” Arm Architecture Reference Manual: Armv8, for A-profile architecture, D4.1.1 “Form of the memory system architecture.” (ARM_0132149 at -782.)

⁵⁴ (QCARM_3087757 at -922.)

⁵⁵ *Id.* at -773.

[REDACTED]

131. As the above shows, Nuvia developed the [REDACTED] core to ultimately be an [REDACTED]. As Mr. Grisenthwaite stated during our conversation, an Arm-compliant core is necessarily [REDACTED] [REDACTED] the Arm architecture. He maintained that one cannot produce an Arm-compliant core without understanding the Arm architecture, which requires consulting the Arm ARM to get every one of thousands of details right. [REDACTED]

[REDACTED]

(iii) [REDACTED]

132. [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED] [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

133. [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]


[REDACTED]

[REDACTED] [REDACTED]

134. [REDACTED]

[REDACTED]

[REDACTED]

Source	File Name	Date	Total Pages	 - Page Numbers
[REDACTED]	[REDACTED]	[REDACTED]	[REDACTED]	[REDACTED]

Source	File Name	Date	Total Pages	“Armv8 ISA support” – Page Numbers
[REDACTED]	[REDACTED]	[REDACTED]	[REDACTED]	[REDACTED]
[REDACTED]	[REDACTED]	[REDACTED]	[REDACTED]	[REDACTED]
[REDACTED]	[REDACTED]	[REDACTED]	[REDACTED]	[REDACTED]
[REDACTED]	[REDACTED]	[REDACTED]	[REDACTED]	[REDACTED]
[REDACTED]	[REDACTED]	[REDACTED]	[REDACTED]	[REDACTED]
[REDACTED]	[REDACTED]	[REDACTED]	[REDACTED]	[REDACTED]
[REDACTED]	[REDACTED]	[REDACTED]	[REDACTED]	[REDACTED]
[REDACTED]	[REDACTED]	[REDACTED]	[REDACTED]	[REDACTED]
[REDACTED]	[REDACTED]	[REDACTED]	[REDACTED]	[REDACTED]

- c. Nuvia utilized Arm materials to develop the [REDACTED] Core.
- (i) Nuvia used [REDACTED] as defined in the ALA Annex to build the [REDACTED] Core.

135. [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED] I understand that Nuvia downloaded these documents and tools either online or through [REDACTED]

[REDACTED] and used

them during the development process for the [REDACTED] core. (*See e.g.*,

ARM_00002045 (showing that [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

136. [REDACTED]

[REDACTED]

[REDACTED] As summarized by Mr. Grisenthwaite during
our conversation, [REDACTED]

[REDACTED] [REDACTED]
[REDACTED]
[REDACTED]
[REDACTED]
[REDACTED]
[REDACTED]
[REDACTED]
[REDACTED]
[REDACTED]
[REDACTED]
[REDACTED]
[REDACTED]
[REDACTED]
[REDACTED]
[REDACTED]

137. [REDACTED]

[REDACTED]
[REDACTED]
[REDACTED]
[REDACTED]

[REDACTED] I further discuss
these verification tools and Nuvia's use of them below in § IV.A.3.a.

138. [REDACTED]

[REDACTED]
[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED] Nuvia downloaded elements of the

[REDACTED]

[REDACTED] [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED] [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

(ii) Nuvia also used other Arm documents, tools, and knowledge to build the [REDACTED] Core.

139. In addition to the [REDACTED] defined in the ALA Annex, Nuvia also used other Arm materials to develop [REDACTED] According to

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED] Most of these files were downloaded in 2019 and 2020, prior to Qualcomm's acquisition of Nuvia. (*See id.*) For example, Mr. Trivedi

downloaded [REDACTED]

(*Id.*; [REDACTED]

) [REDACTED]

[REDACTED] Nuvia engineers Vinod Chamarty and Geeta Balakrishnan

downloaded hundreds of Arm documents and tools while at Nuvia in 2019 and 2020. (*See* ARM_00002045.)

140. Aside from distinct Arm materials and tools, Nuvia also obtained Arm support and knowledge to develop the [REDACTED] core. (*See, e.g.*, ARM_00040395; ARM_00038935.) During my conversation with Mr. Grisenthwaite, he mentioned that [REDACTED]

[REDACTED] In 2020 and 2021, Nuvia/Qualcomm and Arm personnel

[REDACTED]

[REDACTED]

- d. Nuvia and Qualcomm employees testified that the [REDACTED] Cores were designed to implement Armv8 Architecture and be Arm-compliant.

141. [REDACTED]

[REDACTED]

[REDACTED]

142. [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

143. [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

144.

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

145.

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

146.

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

147.

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

148.

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

3. The Nuvia [REDACTED] Core Was Validated as an [REDACTED].

a. Nuvia and Qualcomm used confidential Arm tools to verify the Nuvia [REDACTED] Core's compliance with Armv8 Architecture.

149. In designing the Nuvia [REDACTED] core to be an Arm-compliant core, Nuvia had access to and utilized confidential Arm tools. [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED] [REDACTED] [REDACTED] [REDACTED]. ([REDACTED]

[REDACTED])

150. The [REDACTED], is [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED] [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

151. The [REDACTED] is [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

152. [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

153. [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

b. Arm validated the Nuvia [REDACTED]
Core as an Arm

[REDACTED]

154. [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

155. [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

B. Nuvia's Design of the [REDACTED] Core Is Incorporated into Several of Qualcomm's SoC Products.

156. As I explained in §§ III.C.1 and IV.A above, Nuvia worked on designing and developing a custom Arm CPU core called [REDACTED] which Nuvia worked to incorporate into an SoC called [REDACTED]. As I also explained in § III.C.3, after Qualcomm acquired Nuvia, Qualcomm incorporated the Nuvia [REDACTED] core into several of its SoCs, including the [REDACTED] [REDACTED] SoCs. This is confirmed by the RTL code analysis described below.

157. I understand based on information from Qualcomm's attorneys (*see* 9/12/2023 email from J. Braly to F. Patel) and my own review of the RTL code that Qualcomm has produced the following RTL code in this litigation:

- [REDACTED] NCC
 - March 14, 2021
 - February 28, 2022
 - April 1, 2022
 - October 24, 2022
- [REDACTED] NCC
 - July 30, 2021
 - April 13, 2023
 - October 24, 2023
- [REDACTED] NCC

- January 11, 2022
- July 28, 2023
- [REDACTED] NCC
 - February 21, 2023
 - July 28, 2023
- [REDACTED] NCC
 - July 28, 2023

158. Based on my review, I understand that the RTL code produced for “[REDACTED] NCC,” “[REDACTED] NCC,” “[REDACTED] NCC,” and “[REDACTED] NCC” includes code for versions of the [REDACTED] core incorporated into each of those SoCs. I understand that the RTL code produced for “[REDACTED] NCC” includes code for a CPU core called “[REDACTED]” that is designed [REDACTED]

[REDACTED]

159. I note that the March 14, 2021 [REDACTED] NCC code is dated one day before the March 15, 2021 Qualcomm acquisition of Nuvia. Based on these dates, I understand that the March 14, 2021 [REDACTED] NCC code is RTL code that Nuvia prepared and that Qualcomm acquired as part of its purchase of Nuvia.

160. I understand that Arm asked Dr. Mike Chen to review the RTL source code produced by Qualcomm and prepare an expert report describing his analysis. Dr. Chen is a professor in the School of Electrical and Computer Engineering at the University of Southern California and has a Ph.D. in Electrical Engineering from the University of California at Berkeley.

161. I have reviewed Dr. Chen's expert report. In addition, on December 15 from approximately 9 a.m. to 4:30 p.m., I reviewed the source code produced by Qualcomm on the source code desktop, together with Dr. Chen. During that meeting, Dr. Chen showed me the source code produced by Qualcomm, explained the analysis that he performed, and described his findings.

162. As explained in § II, I am an expert in computer engineering and microprocessor design due to, among other things, my time as Chief Architect of the x86 at Intel. I have extensive experience writing and interpreting RTL. Based on my experience, my review of Dr. Chen's report, my discussions with Dr. Chen, and my own review of the RTL source code, I endorse the qualitative and quantitative conclusions from Dr. Chen's expert report, namely that: [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

163. Specifically, I endorse and share Dr. Chen's conclusion that the

[REDACTED]

[REDACTED]

As Dr. Chen notes in his report, and consistent with my review of

[REDACTED]

As Dr. Chen's report shows, [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

164. I endorse and share Dr. Chen's conclusions that [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED] Using file comparison tools, Dr. Chen was able to show the percentage of [REDACTED] lines of code that precisely matched those in the Nuvia [REDACTED] design. If only a relatively few lines of code were found to have been "reused" from the earlier [REDACTED] RTL, then further investigation would have had to be performed

before concluding that the later designs were the same core as the earlier ones. [REDACTED]

[REDACTED]

165. Dr. Chen also collected data comparing the Nuvia [REDACTED] database to [REDACTED] and [REDACTED] which [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

166. Thus, in view of Dr. Chen's report and my own scrutiny of the RTL code, it is my opinion that the March 14, 2021, Nuvia [REDACTED] code is

[REDACTED]

[REDACTED] Nuvia and Qualcomm designs

after the March 14, 2021, Nuvia [REDACTED] code are also [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

167. In view of Dr. Chen's report and my own code review, it is also my opinion that the March 14, 2021, [REDACTED] code is also [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

C. Qualcomm's Purported Swap Out [REDACTED]

1. Qualcomm's Swap Out Was in Response to Termination of the Nuvia Agreements

168. As discussed in § IV(A), the Nuvia [REDACTED] core was designed to be an [REDACTED]. I understand that, following Arm's termination of the Nuvia ALA and TLA on March 1, 2022, Qualcomm made efforts [REDACTED]

[REDACTED] I refer to this exercise as the "Swap Out," consistent with Qualcomm's terminology. ([REDACTED]

[REDACTED]) I have reviewed Qualcomm's responses to Arm's Interrogatory No. 5 in which Qualcomm describes the actions it undertook as part of the Swap Out.

169. I understand that when Arm terminated the Nuvia ALA and TLA, Arm asked Nuvia to [REDACTED]

[REDACTED] I understand that this language is based on [REDACTED] of the Nuvia ALA and TLA.

(ARM_00059183; ARM_00002988.) By its request, Arm was asking Nuvia to:

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

170. [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

171. [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

2. **The Swap Out** [REDACTED]
[REDACTED]

172. [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED] [REDACTED] [REDACTED] [REDACTED]

[REDACTED]

173. [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED] [REDACTED]

174. [REDACTED]

[REDACTED]

[REDACTED]

175. [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED] [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

176.

[REDACTED]

[REDACTED]

[REDACTED]

**3. Qualcomm Did Not Discontinue Using the
[REDACTED] Cores in [REDACTED]
[REDACTED] Following the Termination of
the Nuvia Licenses**

177. Qualcomm states that it performed the Swap Out to “comply with the termination provisions in Nuvia’s license agreements” (ECF No. 18 at ¶ 231), but the Swap Out [REDACTED]

[REDACTED]

[REDACTED]

178.

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

179. As discussed in § IV.A above, the Nuvia [REDACTED] core was developed as an [REDACTED] based on information in the [REDACTED] and other [REDACTED] materials supplied to Nuvia under the Nuvia ALA.

180. [REDACTED]

[REDACTED]

[REDACTED] Nuvia employees received this information. For example, a download log shows that [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

Transaction ID		Part ID		ALA Annex Part	
[REDACTED]	[REDACTED]	[REDACTED]	[REDACTED]	[REDACTED]	[REDACTED]
	[REDACTED]		[REDACTED]		[REDACTED]
	[REDACTED]		[REDACTED]		[REDACTED]
	[REDACTED]		[REDACTED]		[REDACTED]
	[REDACTED]		[REDACTED]		[REDACTED]

181.

[illegible]

182.

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

V. CONCLUSION

183. My opinions above are based on available information to date. I reserve the right to supplement or amend my opinions in this report, and also

to rebut opinions by Qualcomm's experts with which I disagree. I also reserve the right to correct any clerical errors that I discover after service of this report.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct. Executed on this 20th day of December of 2023 in Portland, Oregon.

By: 

Dr. Robert P. Colwell

APPENDIX A
LIST OF MATERIALS CONSIDERED

All documents cited within this report.

Technical Expert Report of Dr. Michael Chen.

Qualcomm Source Code computer.

Correspondence dated 10/26/2023, email from J. Braly to J. Li.

Correspondence dated 9/12/2023, email from J. Braly to F. Patel.

PLEADINGS

Arm Ltd. v. Qualcomm Inc. et al., No. 1-22-cv-001146 MN (D. Del.):

ECF No. 1, Complaint, dated August 31, 2022.

ECF No. 12, SEALED Defendants' Answer and Defenses to Plaintiff's Complaint and Jury Demand and Defendants' Counterclaim, dated September 30, 2022.

ECF No. 18, SEALED Defendants' Answer and Defenses to Plaintiff's Complaint and Jury Demand and Defendants' Amended Counterclaim, dated October 26, 2022.

ECF No. 23, SEALED Plaintiff Arm Ltd.'s Answer and Affirmative Defenses to Defendants Qualcomm Inc., Qualcomm Technologies, Inc., and Nuvia, Inc.'s Amended Counterclaim, dated November 15, 2022.

DISCOVERY

Defendants' Response and Objections to Plaintiff's First Set of Interrogatories (Nos. 1-13), dated February 27, 2023.

DEPOSITION TRANSCRIPTS REVIEWED⁵⁷

Gulati Deposition Transcript dated October 12, 2023.

Amon Deposition Transcript dated November 15, 2023.

Trivedi Deposition Transcript dated October 25, 2023.

Williams Deposition Transcript dated November 3, 2023.

Asghar Deposition Transcript dated November 8, 2023.

Grisenthwaite Deposition Transcript dated November 15, 2023.

Bos Deposition Transcript dated November 29, 2023.

Thompson Deposition Transcript dated November 28, 2023.

Sharma Deposition Transcript dated October 27, 2023.

Kanopathipillai Deposition Transcript dated December 1, 2023.

PRODUCED MATERIALS

ARM_01324149

ARM_00051126

QCARM_3087757

ARM_00059183

ARM_00057230

QCARM_3087992

ARM_00002988

QCARM_3861394

QCARM_0325086

QCARM_0339310

QCARM_2402257

QCARM_0490031

⁵⁷ I had all deposition transcripts available to me.

QCARM_3088245	QCARM_7403869	ARM_00002516
QCARM_3089361	QCARM_3535060	ARM_00042794
QCARM_3087396	QCARM_3534786	ARM_00038568
QCARM_3088553	QCARM_0338883	ARM_01309676
QCARM_0325371	QCARM_0557206	QCARM_0000864
QCARM_0490329	QCARM_3433989	QCARM_2540979
QCARM_3088937	QCARM_2402586	QCARM_2414840
QCARM_3536689	QCARM_0190735	ARM_00039434
QCARM_3536628	QCARM_3041647	ARM_00001456
QCARM_2423540	ARM_01216002	ARM_00099622
QCARM_3443782	ARM_01230173	QCARM_0337839
QCARM_0027987	QCARM_0181949	QCARM_0338297
QCARM_0339647	QCARM_0182011	ARM_00045395
QCARM_0339935	QCARM_0169739	ARM_00002654
QCARM_0339630	QCARM_0550518	QCARM_3520804
QCARM_3451883	QCARM_3314892	
QCARM_3972047	QCARM_0002581	
QCARM_3535531	ARM_00002045	
QCARM_3535726	ARM_00040395	
QCARM_3535496	ARM_00038935	

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Appendix B

ROBERT P. COLWELL

3594 NW BRONSON CREST LOOP
PORTLAND, OR 97229
503-629-9638
BOB.COLWELL@GMAIL.COM

PROFESSIONAL EXPERIENCE

- **Director**, Microsystems Technology Office, DARPA Arlington VA 2012-2014
- **Deputy Director**, Microsystems Technology Office, DARPA 2011-2012
Led office of 17 program managers, budget ~\$600M/yr, funding research on computer systems, nanophotonics, bioengineering, radar, comms, lasers, IR imaging, and much more.
- **Consultant**, Portland, OR 2001-2011, 2014 - present
General computer HW/SW consulting to industry and academia (Safeware, the University of Pittsburgh, Intel, Qualcomm, venture capital companies, many startups, expert witness engagements, Lawrence Berkeley National Lab, US DoD)
- Named an **Intel Fellow** (27 Fellows in Intel's employee population of ~80,000) in 1997; winner of 2005 **Eckert-Mauchly Award**, highest award in field of computer architecture, for "outstanding achievements in the design and implementation of industry-changing microarchitectures, and for significant contributions to the RISC/CISC architecture debate"; elected to **IEEE Fellow** and **the National Academy of Engineering** in 2006 (the highest recognition in field of engineering) for "contributions to turning novel computer architecture concepts into viable, cutting-edge commercial processors." Inducted into the **American Academy of Arts and Sciences**, 2012. Winner of **IEEE Bob Rau Award**, 2015.
- **Chief IA-32 Architect**, Intel Corporation, Hillsboro OR, 1992-2001
Lead IA32 architect, responsible for all of Intel's x86 Pentium CPU architecture efforts (direct management included 40 – 110 people): Pentium Pro, Pentium II, III, 4; Initiated and led Intel's Pentium 4 CPU development
- **Senior CPU Architect**, Intel Corporation, Hillsboro OR, 1990-1992
One of three senior architects responsible for conceiving Intel's P6 microarchitecture, the core of the company's Pentium II, Pentium III, Celeron, Xeon, and Centrino families
- **Hardware Architect**, Multiflow Computer, New Haven, CT 1985-1990
One of seven hardware engineers who created the world's first VLIW (very long instruction word) scientific supercomputer under direction of Josh Fisher
- **Hardware Engineer** (part-time) Perq Systems, Pittsburgh PA, 1980 - 1984
Hardware design engineer working on graphics display hardware for first generation bit-slice-based engineering workstations
- **Member of Technical Staff**, Bell Telephone Laboratories, Holmdel, NJ, 1977-1980
Hardware design engineer working on 8 and 32-bit microprocessors

EDUCATION

- **PhD in Computer Engineering**, Carnegie-Mellon University, 1985
- **MSEE** in Computer Engineering, Carnegie-Mellon University, 1978

- **BSEE** in Electrical Engineering, University of Pittsburgh, 1977

PUBLICATIONS

Wrote foreword to "Weaving High Performance Multi-Core Processor Fabric: Essential Insights to the Intel Quickpath Architecture", Maddox, Singh, Safranek, Intel Press 2009

National Research Council, The Future of Computing Performance: Game Over or Next Level?, Washington, D.C.: The National Academies Press, 2010.

VLIW: The Unlikeliest Architecture, IEEE Solid State Circuits News, 2009

Wrote intro to DE Shaw's article on the Anton molecular folding engine in CACM, July 2008

Contributed parameterized chapter 2 problem sets to Hennessy & Patterson's "Computer Architecture: A Quantitative Approach, 4th Edition" 2006

The Pentium Chronicles, IEEE/Wiley, December 2005

IEEE Computer Magazine, 48 columns for "At Random" column 2002-2005

Wrote foreword to Josh Fisher's book "Embedded Computing: A VLIW Approach to Architecture, Compilers and Tools", Morgan-Kaufman 2005

We May Need A New Box, IEEE Computer March 2004

Superscalar Processor Design, P6 chapter, Shen & Lipasti, McGraw-Hill 2003

Embedded Everywhere, National Academy of Science, October 2001

Intel's College Hiring Methods and Recent Results, Microelectronics Systems Education Conference, Robert Colwell, Gary Brown, Frank See, July 1999

Microprocessor, Wiley & Son Technical Encyclopedia, 1999

Challenges and Trends in Processor Design, roundtable discussion in IEEE Computer, January 1998

A 0.6um BiCMOS Processor with Dynamic Execution, Robert P. Colwell, Randy L. Steck, 1995 IEEE International Solid State Circuits Conference, pp. 176-177 (won best paper award)

Latent Design Faults in the Development of Multiflow's TRACE/200, 22nd Annual International Symposium on Fault-Tolerant Computing, Boston MA, July 1992

Architecture and Implementation of a VLIW Supercomputer, Robert P. Colwell, W. Eric Hall, Chandra S. Joshi, David B. Papworth, Paul K. Rodman, James E. Tornes, Proceedings of Supercomputing '90, New York, November 1990

A VLIW Architecture for a Trace Scheduling Compiler, Robert P. Colwell, Robert P. Nix, John J. O'Donnell, David B. Papworth, Paul K. Rodman, IEEE Trans. on Comp., V. 37, N. 8, Aug.1988

A VLIW Architecture for a Trace Scheduling Compiler, Robert P. Colwell, Robert P. Nix, John J. O'Donnell, David B. Papworth, Paul K. Rodman, Proceedings of the 2nd Int'l Conf. on

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Fast Object-Oriented Procedure Calls: Lessons from the Intel 432, Edward F. Gehringer, Robert P. Colwell, ISCA 13, June 1986, pp. 92-101

The Performance Effects of Architectural Complexity in the Intel 432, Robert P. Colwell, Edward F. Gehringer, E. Douglas Jensen, ACM Transactions on Computer Systems, Aug. 1988, V. 6, N. 3

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Computers, Complexity, and Controversy, R.P. Colwell, C.Y. Hitchcock III, E.D. Jensen, H.M. Brinkley Sprunt, C.P. Kollar, IEEE Computer, September, 1985, pp. 8-19

The Performance Effects of Function Migration and Architectural Complexity in Object-Oriented Systems, Robert P. Colwell, PhD thesis, Carnegie-Mellon University, Pittsburgh, PA, August 1985

Peering Through The RISC/CISC Fog: An Outline Of Research, Computer Architecture News, Vol. 11, No. 1, March 1983 pp. 44-50

A Perspective on the Processor Complexity Controversy, Proceedings of the International Conference on Computer Design, 1983, pp. 613-616

The Origin of Intel's Micro-ops, invited paper, IEEE Micro 2021

LECTURES AND INVITED TALKS

P6: Myths and Pipelined Realities, MP Forum '95 in Santa Clara

Evolution of Slot 1 and Slot 2, MP Forum '97 in Santa Clara

Micro '30 keynote speaker, 1997, San Jose

HPCA2 keynote speaker, Santa Clara, 1996

Talks on computing futures at CMU and Oregon Graduate Institute, Intel's Design Test and Technology Conference 1997-1998 (best presentation DTTC), invited keynote DTTC '04

LCPC (Languages and Compilers for Parallel Computing) keynote speaker, San Jose 1996

Intel Research Forum invited speaker, Hillsboro '96, Santa Clara '99

Intel Distinguished Lecture Series talks on the Pentium Pro at BYU, MIT, UCB, Stanford, CMU, Illinois, Wisconsin, Univ of Washington, OGI, UCLA

Distinguished Lectures: UC Davis May 2003; Carnegie-Mellon Univ Nov. 2003; USC April 2004

Microprocessor Report dinner speaker on Pentium Pro, March '95

Neural Networks for Computing Conference, Snowbird Utah, April 1994

IEEE Winter VLSI Workshop 1995

DARPA Winter PI conference, Pasadena CA, January 1994

International Applications Conference, San Diego CA, June 1994

Nature's Paradigm and the Challenge of Validation, Intel Validation Summit 1998, invited talk

Validation Lessons from Elsewhere, Intel Validation Summit 1999, invited talk

ISCA keynote, Anchorage Alaska, June 2002

ECE380 Seminar invited talk, Stanford Univ. February 2004

Invited speaker, Technology Management Lecture Series, PSU May 2004

Invited speaker, CSE Division Wide Seminar, University of Michigan, January 2005

Invited keynote speaker, IEEE Int'l Symp. on Async Circuits and Systems, NYC, March 2005

Invited speaker, IEEE Management Series, Portland OR, April 2005

Eckert-Mauchly Award acceptance speech, ISCA, Madison Wisconsin, June 2005

Invited keynote, International Multiconference on Computer Science and Computer Engineering, Las Vegas NV, June 2005

Invited speaker: Google, Sun Labs, Portland State University 2005

Invited speaker: Cadence, Carnegie-Mellon Univ. CS, Univ. of Rochester, Walla Walla College 2006

Invited keynote, PICMET, Portland Oregon, August 2005

Distinguished lecture, Univ. of Utah, March 2006

Invited speaker: Computer Science Symposium, St. Petersburg, Russia 2006

Invited speaker, IEEE-CS 60th anniversary meeting, Santiago Chile, San Diego CA 2006

Invited speaker, National Academies "Distinguished Voices" lecture series, April 2007, Irvine CA

Invited speaker, FCRC "Future Of Computer Architecture 2007", June, San Diego CA

Invited keynote speaker, ASAP 2007 conference, July, Montreal Canada 2007

Invited speaker, UC Irvine, "How To Be a Successful Engineer", Feb. 2008

Invited speaker, US Naval Workshop on Ship Design, Williamsburg, VA May 2008

Invited speaker, DARPA DSRC summer session, Santa Cruz CA July 2008

Distinguished Hopeman Lecture, Grove City College, April 2009

Many invited talks as DARPA MTO spokesperson on the end of Moore's Law 2011-2014

Invited speaker, Microsoft Research 20th Anniversary Symposium, Sept. 2011

Invited speaker, Computer Science and Telecommunications Board (CSTB), Sept. 2011

Invited speaker, Secretary of Defense Corporate Fellows, July 2012, 2013

Invited speaker after-dinner talk, Salishan Conference on High Performance Computing, April 2013

Invited speaker, Industrial Physics Forum, Baltimore MD, March 2013

Invited speaker, Computing Community Consortium (CCC), Pgh PA, March 2013

Invited speaker, National Defense University College, Wash. DC, May 2013

Invited speaker, Design Automation Conference, Austin TX, June 2013

Invited keynote, Hot Chips Conference, Stanford, August 2013

Invited speaker, Gov't Forum on Moore's Law, Wash. DC, November 2013

Invited talks at UT Austin, seminar & computer architecture lecture, November 2013

Invited speaker, Rebooting Computing, Wash. DC, December 2013

Invited speaker, Dartmouth College, January 2014

Invited speaker, MIT Annual Research Conference (MARC), January 2014

Invited speaker, Virginia Tech Univ., February 2014

Invited speaker, Univ. of Rochester, March 2014

Invited speaker, IEEE Technology Time Machine conf, October 2014

Invited speaker, DARPA HAPTIX kickoff meeting, Arlington VA, Nov. 2014

Invited speaker, CSTB Continuing Innovation in IT workshop, Washington DC, Mar. 2015

Invited keynote, Stanford SystemX "Headlights" Workshop, April 2015

Invited keynote, Berkeley Energy Efficient Electronics Systems Symposium, Oct. 2015

Invited speaker, University of Washington, Nov. 2015

Invited speaker, Arizona State University, Feb. 2016

Invited keynote, DoE Extreme Heterogeneity workshop, January 2018

Invited keynote, DARPA NICE workshop, Feb. 2018 (Neuro-Inspired Computing Elements), Oregon

Invited keynote, ModSim workshop, Seattle, August 2018

ECE Commencement speaker, Portland State University, June 2019

Member, National Academy of Engineering review panel for NIST (National Institute of Standards and Technology) Nanotechnology Division, June 2021

Invited keynote, ModSim workshop, Seattle, August 2023

PANEL SESSIONS

DAC '91 panel session panelist; DAC '92 CAD tools workshop instructor

ICCD '91 moderator/organizer of panel session, San Jose CA

ICCAD-94, panel session panelist, November 1994, San Jose CA

Micro 26 '93, moderator/organizer of panel session, Portland OR

ISCA workshop talk, Santa Margherita Ligure, Italy 1995, panelist Phila. PA 1996

PAID 97 Workshop talk on "accidental performance decisions" with Dave Papworth

FPGA panel session panelist, November 1996, Monterey CA

ASPLOS-VII panel session panelist, October 1998, San Jose CA

IEEE Workshop on Low-Power design panel session, San Diego, CA 1999

Four panel sessions in 2000 at various conferences

Computer Research Assoc. "Grand Challenges" conference, Santa Cruz CA, Dec. 2005

DARPA MTO Exposition, Arlington VA July 2014

NSF Future Computing evaluation panel April 2018

ModSim 2018 panelist, Seattle WA

CONFERENCE COMMITTEES

ICCD 1990, 1991, 1992, 1993, 1994, 1995

IEEE Micro 24, 26, 27, 30, 31, 32, general co-chair 37, 39, 40, 41

ISCA 1999, 2000, 2008, 2009, 2010, 2015

Supercomputing 2013, 2014

TECHNICAL EXPERT LEGAL CASES WORKED

AVM v. Intel, Wilmer Hale, Lauren Fletcher, 2015-2017

Damages expert report, deposed, trial Wilmington DE May 2017

Futurelink v. Intel, Kirkland Ellis, Eric Cheng, 2014-2017

Invalidity, non-infringement expert reports, deposed 3 times, case settled 8/17/2023

Broadcom v. Renesas, Morrison Foerster, Fahd Patel, Daniel Muino, 2018-2020

Invalidity, non-infringement expert reports, deposed twice, testified at ITC hearing

Semcon v. Amazon, Sidley Austin, Tung Nguyen, Cal Butcher, 2019

Invalidity expert report, deposed 8/15/19, case settled

VLSI Tech. v. Intel, Wilmer Hale, Christine Duh, George Manley, Jordan Hirsch, 2017-2021

Damages expert report, Rebuttal report, deposed twice

CCO (Computer Circuit Operations) v Marvell, Sheppard Mullin, Wendy Cheung, 2020

Declaration filed, case settled August 2020

ACQIS v. Samsung, DLA Piper, Gianni Minutoli, 2021

Claim Construction declaration, deposed twice, case settled Dec. 2021

ACQIS v. Inventec, BlankRome, Greg Hermann, 2022

Damages & apportionment, case settled May 2022

Apple Inc. v. Future Link Systems, Inter Partes Review, EriseIP, Adam Seitz

IPR declaration filed, case settled April 2022

Apple Inc. v. Future Link Systems, Fish Richardson, John Brinkmann

Work on claim construction, case settled April 2022

ACQIS v. Microsoft, DLA Piper, Gianni Minutoli, 2022

Claim Construction declaration, case settled June 2023

OTHER

Selected as member of ISAT (Information Systems Advanced Technology) panel for DARPA, 2006-2009, co-chaired Machine Learning on Multicore 2009 with Carlos Guestrin and Greg Morrisett

Panelist, Dept of Defense Summer Study on Future Technology, summer 1999, Washington DC

CSTB Panelist, National Academy of Science, Networks of Embedded Processors, 1999-2000, Wash. DC

CSTB Panelist, National Academy of Science, Sustaining Growth in Computing Performance, 2006-2011, Wash. DC

IEEE Computer Magazine editor for High Performance Computing, 1995 to 1999

IEEE Computer Magazine editorial board member, Perspectives editor, 1999-present

Reviewer of dozens of technical books for Morgan Kaufmann, Mindshare, Addison-Wesley

Committee member on NSF funding for computer arch futures, Philadelphia, 1996

Intel Innovator's Day finalist '93, judge '95, judge '97

IEEE Senior Reviewer status in 1994, 1995, 1996 (conference papers, books, magazine articles)

Intel P6 public spokesman at dozens of radio, TV, and magazine interviews

Intel Divisional Award 1993 for DFA performance modeling tool

Intel Achievement Award 1996 for Pentium Pro Microarchitecture

CMU Alumni Merit Award, 1996, for technical leadership on Pentium Pro development

ACM Eckert-Mauchly award committee member, 1998-2001

Univ. of Pgh. Distinguished Alumni Award, 2000, for technical leadership on Intel's microprocessors

Univ. of Pgh. University Achievement Award, 2001, for accomplishments in field of Computing

Carnegie-Mellon Distinguished Alumni Fellows Award 2001

PICMET "Medal of Excellence" 2005

Judge for CSIDC (Computer Society Int'l Design Competition) 2005, 2006

Instructor ECE570, Adv. Computer Arch., Oregon State Univ., winter semesters 2000, 2003

Inventor or co-inventor on 40 patents

EXHIBIT 26

HIGHLY CONFIDENTIAL UNDER THE PROTECTIVE ORDER

Page 1

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

ARM LTD.,)
)
PLAINTIFF,)
)
VS.) Case No. 22-1146 (MN)
)
QUALCOMM INC., QUALCOMM)
TECHNOLOGIES, INC., and)
NUVIA, INC.,)
)
DEFENDANTS.)
_____)

VIDEOTAPED DEPOSITION OF DR. ROBERT COLWELL
TRANSCRIPT DESIGNATED HIGHLY CONFIDENTIAL
FRIDAY, JUNE 28, 2024, 9:07 A.M.
LOS ANGELES, CALIFORNIA

Reported by Desiree Cooks, CSR No. 14075
Job No. 6768619
Pages 1 - 271

HIGHLY CONFIDENTIAL UNDER THE PROTECTIVE ORDER

Page 2	Page 4
<p>1 IN THE UNITED STATES DISTRICT COURT</p> <p>2 FOR THE DISTRICT OF DELAWARE</p> <p>3</p> <p>4</p> <p>5 ARM LTD.,)</p> <p>6)</p> <p>7 PLAINTIFF,)</p> <p>8)</p> <p>9 VS.) Case No. 22-1146 (MN)</p> <p>10)</p> <p>11 QUALCOMM INC., QUALCOMM)</p> <p>12 TECHNOLOGIES, INC., and)</p> <p>13 NUVIA, INC.,)</p> <p>14)</p> <p>15 DEFENDANTS.)</p> <p>16 _____)</p> <p>17</p> <p>18</p> <p>19</p> <p>20</p> <p>21 THE VIDEOTAPED DEPOSITION OF DR. ROBERT COLWELL, taken</p> <p>22 at 707 Wilshire Boulevard, 60th Floor, Los Angeles,</p> <p>23 California, on Friday, June 28, 2024, at 9:07 a.m.,</p> <p>24 before Desiree Cooks, Certified Shorthand Reporter, in</p> <p>25 and for the State of California.</p>	<p>1 INDEX</p> <p>2</p> <p>3 WITNESS: DR. ROBERT COLWELL</p> <p>4</p> <p>5 EXAMINATION PAGE</p> <p>6 BY MS. NYARADY 7</p> <p>7</p> <p>8</p> <p>9</p> <p>10 INFORMATION REQUESTED</p> <p>11 PAGE LINE</p> <p>12 (NONE)</p> <p>13</p> <p>14 DOCUMENTS REQUESTED</p> <p>15 PAGE LINE</p> <p>16 (NONE)</p> <p>17</p> <p>18 WITNESS INSTRUCTED NOT TO ANSWER</p> <p>19 PAGE LINE</p> <p>20 57 23</p> <p>21</p> <p>22</p> <p>23</p> <p>24</p> <p>25</p>
Page 3	Page 5
<p>1 APPEARANCES:</p> <p>2 For the Plaintiff:</p> <p>3 MORRISON & FOERSTER LLP</p> <p>4 BY: DANIEL MUINO, ESQ.</p> <p>5 707 Wilshire Boulevard, 60th Floor</p> <p>6 Los Angeles, California 90017</p> <p>7 (650) 813-5688</p> <p>8 Dmuino@mofo.com</p> <p>9</p> <p>10 For the Defendants:</p> <p>11 PAUL WEISS RIFKIND WHARTON & GARRISON, LLP</p> <p>12 BY: CATHERINE NYARADY, ESQ.</p> <p>13 -- JACOB BRALY, ESQ.</p> <p>14 1285 Avenue of the Americas</p> <p>15 New York, New York 10019</p> <p>16 (212) 492-0726</p> <p>17 Cnyarady@paulweiss.com</p> <p>18 Jbraly@paulweiss.com</p> <p>19</p> <p>20 NORTON ROSE FULBRIGHT, LLP</p> <p>21 BY: JOHN POULOS, ESQ.</p> <p>22 1045 West Fulton Street, Suite 1200,</p> <p>23 Chicago, Illinois 60607</p> <p>24 (312) 964-7766</p> <p>25 John.poulos@nortonrosefulbright.com</p> <p>Also present:</p> <p>Jacob Florez, Videographer</p>	<p>1 INDEX TO EXHIBITS</p> <p>2</p> <p>3 EXHIBIT MARKED</p> <p>4 Exhibit QX247 Curriculum Vitae of Dr. Robert 15</p> <p>5 P. Colwell</p> <p>6</p> <p>7 Exhibit QX248 Opening Expert Report of 110</p> <p>8 Dr. Robert P. Colwell</p> <p>9 (Not Attached)</p> <p>10</p> <p>11 Exhibit QX249 Technology License Agreement 172</p> <p>12 between Arm Limited and Nuvia,</p> <p>13 Inc.</p> <p>14</p> <p>15 Exhibit QX250 ANNEX 1 NUVIA ARMV8-A 172</p> <p>16 ARCHITECTURE, Bates</p> <p>17 QCARM_0315570 - 0315583</p> <p>18</p> <p>19 Exhibit QX251 ANNEX 1 NUVIA ARMV8-A 172</p> <p>20 ARCHITECTURE, Bates</p> <p>21 QCARM_0339310 - 0339325</p> <p>22</p> <p>23 Exhibit QX252 Rebuttal Expert Report of 246</p> <p>24 Dr. Robert Colwell to</p> <p>25 Dr. Annavaram's Opening Expert</p> <p>Report</p> <p>(Not Attached)</p> <p>Exhibit QX253 Chat Bates-stamped 255</p> <p>QCARM_0360587</p> <p>Exhibit QX254 Excerpt of Lynn Bos's 255</p> <p>Deposition, dated</p> <p>November 29, 2023</p> <p>PREVIOUSLY MARKED EXHIBITS</p> <p>EXHIBIT IDENTIFIED</p> <p>Exhibit QX242 164</p> <p>Exhibit QX244 167</p>

HIGHLY CONFIDENTIAL UNDER THE PROTECTIVE ORDER

<p style="text-align: right;">Page 6</p> <p>1 FRIDAY, JUNE 28, 2024, 9:07 A.M.</p> <p>2 LOS ANGELES, CALIFORNIA</p> <p>3</p> <p>4 THE VIDEOGRAPHER: This is Jacob Florez, the</p> <p>5 videographer. I represent Veritext Legal Solutions in</p> <p>6 Los Angeles, California. I'm a California notary public,</p> <p>7 number 2365264. I am not financially interested in this</p> <p>8 action, nor am I a relative or employee of any attorney</p> <p>9 or any party.</p> <p>10 Today's date is June 28th, 2024. The current</p> <p>11 time on the monitor is 9:07 a.m. We're on record. This</p> <p>12 deposition is taking place at 707 Wilshire Boulevard,</p> <p>13 Number 6000, Los Angeles, California 90017.</p> <p>14 This is the deposition of Dr. Robert Colwell in</p> <p>15 the matter of Arm Ltd. vs. Qualcomm, Inc., et al. Case</p> <p>16 number: 22-1146 (MN).</p> <p>17 Would counsel please introduce themselves for</p> <p>18 the record.</p> <p>19 MR. MUINO: Daniel Muino of Morrison & Foerster</p> <p>20 for plaintiff, Arm Ltd.</p> <p>21 MS. NYARADY: Catherine Nyarady from Paul Weiss</p> <p>22 for the defendants.</p> <p>23 And I'm joined by my colleague Jake Braly, also</p> <p>24 of Paul Weiss.</p> <p>25 THE VIDEOGRAPHER: Thank you.</p>	<p style="text-align: right;">Page 8</p> <p>1 A No.</p> <p>2 Q Are you purporting to bring any legal expertise</p> <p>3 to these proceedings?</p> <p>4 A No.</p> <p>5 Q Are you intending to give any opinions in terms</p> <p>6 of how to interpret the contracts at issue in this case?</p> <p>7 A Not per se. I do think there's technical</p> <p>8 aspects of what some of those words mean. And I am --</p> <p>9 and I have opined on my -- my position on those in those</p> <p>10 reports.</p> <p>11 Q And you don't --</p> <p>12 You don't intend those to be legal definitions,</p> <p>13 do you?</p> <p>14 A No. I am not a lawyer.</p> <p>15 Q Okay. So if the court were --</p> <p>16 Well, are you aware that it is actually the</p> <p>17 court's job, most often, to interpret a contract?</p> <p>18 A I don't know who interprets contracts like</p> <p>19 that.</p> <p>20 Q Okay. Well, assume -- assume that the judge is</p> <p>21 going to be interpreting at least portions of this</p> <p>22 contract for us. If her interpretation is at odds with</p> <p>23 yours, you will -- you will apply her definitions; right?</p> <p>24 A I believe that's how it works.</p> <p>25 Q When you say "hardware," what does that mean?</p>
<p style="text-align: right;">Page 7</p> <p>1 Will our court reporter please swear in the</p> <p>2 witness.</p> <p>3 DR. ROBERT COLWELL,</p> <p>4 having been first duly sworn, testifies as follows:</p> <p>5 EXAMINATION</p> <p>6 BY MS. NYARADY:</p> <p>7 Q Good morning, Dr. Colwell.</p> <p>8 A Good morning.</p> <p>9 Q You are appearing today and in this case as an</p> <p>10 expert witness; right?</p> <p>11 A Yes.</p> <p>12 Q What is your area of expertise with respect to</p> <p>13 this case?</p> <p>14 A Generally, computer design, including computer</p> <p>15 architecture, microarchitecture, systems, software. The</p> <p>16 list is pretty long.</p> <p>17 Q Is the list included in those general</p> <p>18 categories, or are there other things that you are</p> <p>19 claiming -- or relying on your expertise for this case?</p> <p>20 A Well, the thing -- I didn't say hardware. I'm</p> <p>21 primarily a hardware designer.</p> <p>22 But I don't think -- that doesn't seem to be</p> <p>23 heavily related to the case, so I didn't put it on the</p> <p>24 list, but that's another area that I'm an expert at.</p> <p>25 Q You're not a lawyer, are you?</p>	<p style="text-align: right;">Page 9</p> <p>1 A It -- it varies from circuit level:</p> <p>2 Transistors, wires, components like capacitors,</p> <p>3 resistors.</p> <p>4 Underneath every function that you find in a</p> <p>5 processor, ultimately, there's a circuit somewhere. And</p> <p>6 so my expertise does not extend beyond that down to the</p> <p>7 silicon level.</p> <p>8 There's other people that know how to take</p> <p>9 circuit designs and cache them into transistors and wires</p> <p>10 and things like that. But that's, basically, where my</p> <p>11 expertise starts, is at the hardware level and up- --</p> <p>12 upwards.</p> <p>13 Q You used the word "silicon."</p> <p>14 Is that colloquially used or maybe even more</p> <p>15 technically used in your industry to mean the chip</p> <p>16 itself?</p> <p>17 A That's what I mean by it, yeah. It's --</p> <p>18 because most commercial silicon is composed of silicon at</p> <p>19 its base, there are other chemical -- there are other</p> <p>20 things you can find from the periodic chart that you can</p> <p>21 make chips out of.</p> <p>22 But those tend to be specialty items like what</p> <p>23 the military might use.</p> <p>24 Q Okay. So when people in your field, the</p> <p>25 engineers that have testified in this case, when people</p>

3 (Pages 6 - 9)

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<p style="text-align: right;">Page 10</p> <p>1 say silicon, they mean the chip; right?</p> <p>2 A I assume that's what they mean. That's what I</p> <p>3 mean.</p> <p>4 Q That's how you would understand their use of</p> <p>5 it?</p> <p>6 A Generally, yes.</p> <p>7 Q Okay. Are you a finance or a marketing expert?</p> <p>8 A By no means.</p> <p>9 Q How about a licensing expert?</p> <p>10 A In this case, I'm not acting as a licensing</p> <p>11 expert, no.</p> <p>12 Q Are you an expert in intellectual property?</p> <p>13 A In some respects, yes. I've worked as an</p> <p>14 expert in many cases. And, often, it's a -- I have to</p> <p>15 consider a prior art, for example, or infringement</p> <p>16 aspects. And those do relate to intellectual property.</p> <p>17 Q And in those --</p> <p>18 You're talking about patents mostly; right?</p> <p>19 A Patents, yes.</p> <p>20 Q And in those cases, though, you've served as a</p> <p>21 technical expert; is that right?</p> <p>22 A Technical or fact expert.</p> <p>23 Q Okay. But you've never --</p> <p>24 You're not ever on the legal side of patents or</p> <p>25 patent law? I mean, have you ever testified as a legal</p>	<p style="text-align: right;">Page 12</p> <p>1 A It is a piece of silicon that -- on which the</p> <p>2 manufacturer has already placed some number of</p> <p>3 primitives, where each primitive might be a cell with a</p> <p>4 processor -- a really simple processor -- but a</p> <p>5 processor, some local memory, and some interconnection on</p> <p>6 the chip.</p> <p>7 And the point of an FPGA is you can reprogram</p> <p>8 it to be what you want it to be. So it's kind of a</p> <p>9 hybrid between pure silicon -- a "pure circuit based, you</p> <p>10 know, purpose built, only does one thing" kind of a</p> <p>11 design and a fully general processor.</p> <p>12 Q And for who or which company or in what context</p> <p>13 was the work that you did for the FPGAs?</p> <p>14 A That -- that -- the FPGAs, that was a project</p> <p>15 that I've been involved in since 2005 or so. It's -- I</p> <p>16 don't know how much you want to hear about it.</p> <p>17 Q It's ongoing?</p> <p>18 A Oh, it's ongoing.</p> <p>19 Q I just want to know who it's with? Is there a</p> <p>20 corporate entity?</p> <p>21 A There's no company.</p> <p>22 Q Okay.</p> <p>23 A Yeah, it's a -- well, here's the -- the story</p> <p>24 is I was approached in 2005 by a pianist in Portland,</p> <p>25 Oregon. And he said -- "Bob Moog of Moog synthesizer --</p>
<p style="text-align: right;">Page 11</p> <p>1 expert in those proceedings?</p> <p>2 A I'm not even sure what that means, so probably</p> <p>3 no.</p> <p>4 Q Fair enough. Usually they're excluded anyways.</p> <p>5 A Maybe that's why.</p> <p>6 Q Do you consider yourself an expert in -- in</p> <p>7 RTL? And by "RTL," I mean Register Transfer Language. I</p> <p>8 assume we can use the term "RTL" today.</p> <p>9 A Yes.</p> <p>10 Q Are you an expert in RTL?</p> <p>11 A Yes.</p> <p>12 Q Do you often code an RTL?</p> <p>13 A Nowadays, not so much.</p> <p>14 Q When's -- when was the last period of time that</p> <p>15 you had some consulting or employment where you had to</p> <p>16 code an RTL?</p> <p>17 A Well, one period that I remember -- oh, it</p> <p>18 wasn't my code, but I was looking at RTL for the -- for</p> <p>19 [REDACTED].</p> <p>20 And then there was another -- there are other</p> <p>21 projects that I've worked on that use FPGAs. And those</p> <p>22 are programs in RTL as well.</p> <p>23 Q What are FPGAs?</p> <p>24 A It stands for Field Programmable Gate Array.</p> <p>25 Q And what is that?</p>	<p style="text-align: right;">Page 13</p> <p>1 if you don't know what those are, you've heard them,</p> <p>2 popular music. Beatles used these machines.</p> <p>3 They're keyboards with a mad scientist, kind</p> <p>4 of, you know, a bunch of modules in front of them. And</p> <p>5 it produces music by purely electronic means in a very</p> <p>6 flexible way so you can make all sorts of crazy sounds</p> <p>7 with it.</p> <p>8 In the '60s, Walter Carlos produced an album</p> <p>9 called Switched-On Bach, which was his electronic</p> <p>10 synthesizer rendition of famous Bach tunes. It was a big</p> <p>11 hit at the time.</p> <p>12 Q So you're working on electronics that would be</p> <p>13 used in such keyboards?</p> <p>14 A In that keyboard. It's a very specialized</p> <p>15 keyboard where you're sensing where the finger is</p> <p>16 touching the key.</p> <p>17 Q Okay.</p> <p>18 A And using that -- so it is not a paid position.</p> <p>19 It is a, you know, volunteer thing, but it's a lot of fun</p> <p>20 and it's -- it's that kind of engineering.</p> <p>21 So for a while there, we thought about using</p> <p>22 FPGAs. And we went down that path for a while. And then</p> <p>23 we switched to Arm processors.</p> <p>24 Q Interesting.</p> <p>25 [REDACTED]</p>

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<p style="text-align: right;">Page 14</p> <p>[REDACTED]</p> <p>1 [REDACTED]</p> <p>2 [REDACTED]</p> <p>3 [REDACTED]</p> <p>4 [REDACTED]</p> <p>5 [REDACTED]</p> <p>6 [REDACTED]</p> <p>7 [REDACTED]</p> <p>8 [REDACTED]</p> <p>9 [REDACTED]</p> <p>10 [REDACTED]</p> <p>11 [REDACTED]</p> <p>12 [REDACTED]</p> <p>13 [REDACTED]</p> <p>14 [REDACTED]</p> <p>15 [REDACTED]</p> <p>16 [REDACTED]</p> <p>17 [REDACTED]</p> <p>18 [REDACTED]</p> <p>19 [REDACTED]</p> <p>20 [REDACTED]</p> <p>21 [REDACTED]</p> <p>22 [REDACTED]</p> <p>23 [REDACTED]</p> <p>24 [REDACTED]</p> <p>25 [REDACTED]</p>	<p style="text-align: right;">Page 16</p> <p>1 A I should put a revision number on these things</p> <p>2 because I don't -- I change them and then I can't tell.</p> <p>3 Which one is this?</p> <p>4 Q I will represent that we -- we got this from</p> <p>5 the -- what was attached to your expert report.</p> <p>6 So I guess at that time, did you endeavor to</p> <p>7 provide the most current copy of the CV?</p> <p>8 A I did.</p> <p>9 Q All right. So after you got your Ph.D., it</p> <p>10 looks like you worked at a company called Multiflow</p> <p>11 Computer as a hardware -- as an architect; is that right?</p> <p>12 A Yeah, that's right.</p> <p>13 Q Were you working at all with the Arm</p> <p>14 architecture in this role?</p> <p>15 A I believe Arm had not yet been incorporated as</p> <p>16 of that date, so no.</p> <p>17 Q Okay. And from there you went to Intel; right?</p> <p>18 A Correct.</p> <p>19 Q And you were at Intel through 2001; is that</p> <p>20 right?</p> <p>21 A Yes.</p> <p>22 Q So from 1990 to 2001.</p> <p>23 Were you working with the Arm architecture at</p> <p>24 Intel?</p> <p>25 A Not -- I wasn't personally working with Arm at</p>
<p style="text-align: right;">Page 15</p> <p>[REDACTED]</p> <p>1 [REDACTED]</p> <p>2 [REDACTED]</p> <p>3 [REDACTED]</p> <p>4 [REDACTED]</p> <p>5 [REDACTED]</p> <p>6 [REDACTED]</p> <p>7 [REDACTED]</p> <p>8 [REDACTED]</p> <p>9 [REDACTED]</p> <p>10 [REDACTED]</p> <p>11 [REDACTED]</p> <p>12 [REDACTED]</p> <p>13 [REDACTED]</p> <p>14 [REDACTED]</p> <p>15 [REDACTED]</p> <p>16 [REDACTED]</p> <p>17 MS. NYARADY: Why don't we mark as the next</p> <p>18 exhibit -- this, I believe, was attached to your expert</p> <p>19 report, but I'm just going to mark it separately.</p> <p>20 It's just a copy of your CV, so we're going to</p> <p>21 mark it as QX247.</p> <p>22 (Exhibit QX247 marked.)</p> <p>23 BY MS. NYARADY:</p> <p>24 Q So what I've marked as QX247, that's a copy of</p> <p>25 your -- what should be up-to-date CV; is that right?</p>	<p style="text-align: right;">Page 17</p> <p>1 Intel, no.</p> <p>2 [REDACTED]</p> <p>3 [REDACTED]</p> <p>4 [REDACTED]</p> <p>5 [REDACTED]</p> <p>6 [REDACTED]</p> <p>7 [REDACTED]</p> <p>8 In fact, my understanding was Intel purchased</p> <p>9 that -- whatever that was. But they got Strongarm as</p> <p>10 part of some deal that they did. Yeah, I did notice that</p> <p>11 when I was there.</p> <p>12 Q What do you mean -- well, let's start with:</p> <p>13 What is Strongarm?</p> <p>14 A Strongarm was a version -- I think it's fair to</p> <p>15 say it was a version of the Arm architecture. I don't</p> <p>16 know the particulars. I was designing my own chips at</p> <p>17 the time.</p> <p>18 Q Was it an actual product that was obtained? I</p> <p>19 mean, in terms of, like, a core that was obtained, or are</p> <p>20 you talking about Intel had the rights to develop its own</p> <p>21 core, for lack of a better term?</p> <p>22 A I believe -- well, my understanding at the time</p> <p>23 was that Intel as part of the deal that -- whatever that</p> <p>24 deal was that -- that introduced Strongarm to Intel, I</p> <p>25 believe that they got actual -- an actual core design.</p>

5 (Pages 14 - 17)

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<p style="text-align: right;">Page 110</p> <p>1 THE VIDEOGRAPHER: The time is 11:37 a.m. Off</p> <p>2 record.</p> <p>3 (Break held off the record.)</p> <p>4 THE VIDEOGRAPHER: The time is 11:57 a.m.</p> <p>5 We're back on record.</p> <p>6 MS. NYARADY: So I realized I have not marked</p> <p>7 your report. And I know at times we've been at least</p> <p>8 talking about the opening one. So why don't -- can hand</p> <p>9 me the report that you have in front of you? Thank you.</p> <p>10 And, just for the record, I am going to mark as</p> <p>11 QX248 the opening expert report of Dr. Robert P. Colwell</p> <p>12 served in this case on -- it doesn't have a date on it.</p> <p>13 December --</p> <p>14 THE WITNESS: 12-15, maybe.</p> <p>15 (Exhibit QX248 marked.)</p> <p>16 BY MS. NYARADY:</p> <p>17 Q December 20th -- December 20th of 2023; right?</p> <p>18 Oh, it does have it. It has the date right above your</p> <p>19 signature. Actually, let me open it. So I'm going to</p> <p>20 open it for you, QX248. I'm going to open to Page 96.</p> <p>21 And can you just confirm for me, sir, that that</p> <p>22 is your signature?</p> <p>23 A Yes.</p> <p>24 Q And QX248 is a copy of your opening expert</p> <p>25 report in this case?</p>	<p style="text-align: right;">Page 112</p> <p>1 this case? Right?</p> <p>2 A Right.</p> <p>3 Q Okay. Do you recall which code basis you</p> <p>4 reviewed?</p> <p>5 A You mean, like, directory names or project</p> <p>6 names?</p> <p>7 Q Yeah, or -- let me -- maybe let me make it a</p> <p>8 little bit easier: Your report says that Dr. Chen showed</p> <p>9 you the source code produced and explained his analysis.</p> <p>10 Did you look at any portions of the source code</p> <p>11 beyond the portions that Dr. Chen talks about in his</p> <p>12 expert report?</p> <p>13 A Oh, we did -- we did a fair amount of</p> <p>14 searching. And not all of that resulted in something</p> <p>15 worth putting in this report. I -- I don't remember any</p> <p>16 specifics, but that's -- that's generally how I remember</p> <p>17 the meeting going.</p> <p>18 Q Were you actually doing Beyond Compare</p> <p>19 comparisons during this day in the code room?</p> <p>20 A Yes.</p> <p>21 Q You personally did them?</p> <p>22 A Well, sitting next to him, we both did them. I</p> <p>23 mean, it was just, "Hey, let's -- let's compare these</p> <p>24 files and see if they're the same."</p> <p>25 Q So Dr. Chen had not done this previous to your</p>
<p style="text-align: right;">Page 111</p> <p>1 A Yes.</p> <p>2 Q Okay. Now, you say in Paragraph 161, if you</p> <p>3 want to take a look at that, you say that you -- on</p> <p>4 December 15th from approximately 9:00 to 4:30 p.m. you</p> <p>5 reviewed source code produced by Qualcomm on the source</p> <p>6 code desktop together with Dr. Chen.</p> <p>7 And during that meeting, "Dr. Chen," you say,</p> <p>8 "showed me the source code produced by Qualcomm,</p> <p>9 explained the analysis that he performed, and described</p> <p>10 his findings."</p> <p>11 Do you see that?</p> <p>12 A Yes.</p> <p>13 Q Other than December 15th referred to in your</p> <p>14 Paragraph 161, did you at any other time go to the</p> <p>15 location of the Qualcomm source code to review the</p> <p>16 Qualcomm source code?</p> <p>17 A No. That was the only time.</p> <p>18 Q Okay. And that process, there's a location --</p> <p>19 right? -- where you have to go to review the source code?</p> <p>20 A Yes.</p> <p>21 Q Like a third-party vendor location?</p> <p>22 A I believe it was, yes.</p> <p>23 Q Okay. And it's -- there's a specific room.</p> <p>24 And is it -- it just like a desktop computer that you</p> <p>25 have access to the source code that's been produced in</p>	<p style="text-align: right;">Page 113</p> <p>1 --</p> <p>2 A Oh, he might have. I mean, I am not aware of</p> <p>3 all of the things he did before I showed up on that</p> <p>4 particular day.</p> <p>5 But I -- I know that I instituted -- that's not</p> <p>6 the right word -- instigated certain file comparisons</p> <p>7 because I was just curious. I mean, it just popped up</p> <p>8 during talking to him.</p> <p>9 Q Because the paragraph says that Dr. Chen</p> <p>10 explained the analysis that he had performed.</p> <p>11 So that language made me think that he had</p> <p>12 already done comparisons and he was showing you, maybe,</p> <p>13 how he did it or what he did.</p> <p>14 Did that happen?</p> <p>15 A It did, yeah. He did do that.</p> <p>16 Q Okay. But then you're saying there were other</p> <p>17 comparisons that were run that day?</p> <p>18 A Yes.</p> <p>19 Q Beyond what he had already done?</p> <p>20 A Correct, yeah. I was asking questions. And</p> <p>21 sometimes the easiest way to answer it is to let your</p> <p>22 fingers do the talking.</p> <p>23 Q Did any of those comparisons end up in your</p> <p>24 expert report?</p> <p>25 A Are you talking about -- which -- the opening</p>

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<p style="text-align: right;">Page 114</p> <p>1 report?</p> <p>2 Q Yes. And I'm not trying to be tricky. I</p> <p>3 haven't seen any. So I'm just trying to understand, kind</p> <p>4 of, the --</p> <p>5 Whatever additional comparisons that you may</p> <p>6 have run, would those be comparisons that we then see in</p> <p>7 Dr. Chen's report as the RTL analysis?</p> <p>8 Or is there something in your report that</p> <p>9 you're referring to when you say that you did these --</p> <p>10 these comparisons or analyses, if you will, beyond, you</p> <p>11 know, what Dr. Chen had done?</p> <p>12 A Man, it's been a while, but the main thing I</p> <p>13 remember coming up in that regard was that I said, "Well,</p> <p>14 can we just check and see if the word 'NOVIA' appears in</p> <p>15 the source code for [REDACTED]?" for example, and he said,</p> <p>16 "Sure."</p> <p>17 So I don't remember at the moment whether I put</p> <p>18 that in my report or if he put it in his, but that's one</p> <p>19 of the things I remember doing.</p> <p>20 Q Okay. Anything else that you recall that was</p> <p>21 something that was done that was not done by Dr. Chen,</p> <p>22 you know, himself previous to your visit with Dr. Chen?</p> <p>23 A There -- so on the qualitative part, we spent</p> <p>24 part of the day looking for places where it would be</p> <p>25 clear that there was something in the RTL that is</p>	<p style="text-align: right;">Page 116</p> <p>1 that I mentioned a minute ago, where you look for</p> <p>2 features and, like, what is [REDACTED]? What do they do with</p> <p>3 it in the RTL? Oh, look at that. It's the same bit as</p> <p>4 the Arm ARM says to set.</p> <p>5 Q Before December 15th and the code room, had you</p> <p>6 used Beyond Compare?</p> <p>7 A Yes.</p> <p>8 Q How familiar with Beyond Compare were you</p> <p>9 before December 15th of 2023?</p> <p>10 A Pretty familiar. I mean, I've used it in other</p> <p>11 cases and other experts have used it in other cases. And</p> <p>12 I had analyzed what they were doing.</p> <p>13 Q Are you familiar with all of the standard</p> <p>14 parameter settings for Beyond Compare?</p> <p>15 A I'm mostly familiar with the -- whatever they</p> <p>16 call SKU tolerance, I think, the window that he used, how</p> <p>17 far away do you look for similar lines.</p> <p>18 Q Are there any other standard parameter settings</p> <p>19 that you're aware of?</p> <p>20 A Not offhand, no. That's the one I pay the most</p> <p>21 attention to.</p> <p>22 Q Did you or Dr. Chen change any settings, any of</p> <p>23 the standard settings, on the 15th, December 15th, when</p> <p>24 you were looking through the code?</p> <p>25 A I don't think so. My best recollection is he</p>
<p style="text-align: right;">Page 115</p> <p>1 attributable back to the Arm ARM, for instance. And</p> <p>2 so -- and he -- and he said, "Yes, I've done some of that</p> <p>3 already and here's what I looked for and here's what I</p> <p>4 found."</p> <p>5 And we did a little bit of looking around on</p> <p>6 that subject as well.</p> <p>7 Q To the extent that you located anything, as you</p> <p>8 said, attributable to the Arm ARM, I take it that either</p> <p>9 you or Dr. Chen would have endeavored to put that in the</p> <p>10 report if, in fact, it's an opinion that you're going to</p> <p>11 offer in this case; right?</p> <p>12 A I would hope so, sure, yeah.</p> <p>13 Q Okay. You say that he explained to you the</p> <p>14 analysis that he had performed.</p> <p>15 What do you mean by that?</p> <p>16 A He described to me the basic approach that he</p> <p>17 was taking to -- to answering the question of what is</p> <p>18 there -- is there a family lineage here that can be</p> <p>19 established or are there files identical before and after</p> <p>20 acquisition?</p> <p>21 And so that was the kind of -- does it call it</p> <p>22 quantitative?</p> <p>23 Q Yes.</p> <p>24 A But it's the part where you do file</p> <p>25 comparisons. And then there was the qualitative part</p>	<p style="text-align: right;">Page 117</p> <p>1 fired up the tool, fed in the files, and looked at the</p> <p>2 results.</p> <p>3 Q Okay. What did you do to prepare for your</p> <p>4 deposition today?</p> <p>5 A On my own, I re- -- I went back over my</p> <p>6 reports. I looked at some of Dr. Annavaram's -- I said</p> <p>7 it wrong again, didn't I?</p> <p>8 Q Although, you know, I suppose I could be</p> <p>9 equally wrong. Annavaram.</p> <p>10 A Annavaram. Okay. I'll try to remember.</p> <p>11 I looked at his reports again. I glanced -- I</p> <p>12 at least skimmed over Dr. Chen's reports again. I'm sure</p> <p>13 there was more. Anyway, that was the stuff that I did.</p> <p>14 And then on -- what is today? Friday?</p> <p>15 Q Yes.</p> <p>16 A Yesterday, I met with counsel via telephone --</p> <p>17 Zoom or Webex or Teams or something, online. I met with</p> <p>18 counsel for about four hours -- no, two hours yesterday</p> <p>19 and about four or five hours the day before.</p> <p>20 Q And "counsel," was it all counsel from MoFo?</p> <p>21 A Yes.</p> <p>22 Q Okay. Anything else?</p> <p>23 A I don't know. The odd hour here or there.</p> <p>24 Glancing over -- I mean, there's an awful a lot of cites</p> <p>25 here. I looked at a couple of those again.</p>

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<p style="text-align: right;">Page 118</p> <p>1 Q Did you speak to any Arm employees in 2 preparation for your deposition?</p> <p>3 A No.</p> <p>4 Q Did you speak with Dr. Chen in preparation for 5 your deposition?</p> <p>6 A No.</p> <p>7 Q Did you --</p> <p>8 Have you reviewed Dr. Chen's testimony?</p> <p>9 A Which testimony? His deposition?</p> <p>10 Q Yes.</p> <p>11 A No.</p> <p>12 Q Has anyone spoken to you about Dr. Chen's 13 testimony of a couple days ago?</p> <p>14 A No. I knew that it happened, but I haven't 15 heard anything about it.</p> <p>16 Q So you haven't heard anything substantive?</p> <p>17 A No.</p> <p>18 Q Okay. Yeah, no. I want to talk a little bit 19 more about the ISA. And, again, I think you already said 20 this, but that's an Instruction Set Architecture; right?</p> <p>21 A That's what ISA means, yes.</p> <p>22 Q And that is --</p> <p>23 Well, how would you define an ISA?</p> <p>24 A I think the best quasi definition for ISA is 25 that it represents the interface between the hardware on</p>	<p style="text-align: right;">Page 120</p> <p>1 be the primary concern; right? I mean, those are 2 designer choices of the microarchitecture.</p> <p>3 Is that fair?</p> <p>4 A I think it probably is fair, yeah. Yes. You 5 have -- in general, there is leeway for the design team 6 to steer any given design towards opt- -- towards being 7 optimal for the market in which they hope to compete in.</p> <p>8 Q And the ISA doesn't tell you exactly -- strike 9 that.</p> <p>10 The ISA doesn't tell a microarchitect how to 11 instantiate instructions into the microarchitecture, does 12 it?</p> <p>13 A Only in -- in certain ways it does, but mostly 14 not. "In certain ways" being, for instance, there's an 15 exception model. And things can happen that are 16 extraneous -- that's not even fair.</p> <p>17 Things can happen that are unusual as you're 18 executing code. You might take an interrupt. You might 19 run into a trap. You might do a divide by zero 20 exception.</p> <p>21 If anything funky like that happens, the 22 machine has to react to it in a certain way that's 23 defined by the ISA. So -- so there is that subtle, you 24 know, it isn't just knowing the instructions.</p> <p>25 You also have to know a little bit about how to</p>
<p style="text-align: right;">Page 119</p> <p>1 the one side and the software that's going to run on that 2 hardware on the other side.</p> <p>3 So it's kind of a compact. It's an agreement 4 that the software people will use it in a certain way 5 and, therefore, the hardware people will provide the 6 resources so that the machine will provide that interface 7 that the software people are expecting.</p> <p>8 Q We touched on this a little bit earlier, but 9 the ISA doesn't tell -- tell you, you know, which 10 features to prioritize in the core that you're 11 making; right?</p> <p>12 A I'd need to know what features you're thinking 13 of to answer that.</p> <p>14 Q So isn't the ISA a set of instructions with 15 respect to the architecture features?</p> <p>16 A The ISA will include a set of instructions and 17 include how they're encoded, but it has to be a lot more 18 than that.</p> <p>19 I mean, you also have to know what data types 20 are inside the machine, what the memory access ordering 21 rules are, there's a bunch more.</p> <p>22 Q But I guess I'm focusing on when you're 23 designing a microprocessor, the ISA isn't going to tell 24 you whether you should value power over something else or 25 whether, you know, battery life is something that should</p>	<p style="text-align: right;">Page 121</p> <p>1 handle them when unusual things happen. So there's other 2 subtleties like that.</p> <p>3 Q But, in general, it sounds like you're in 4 agreement that the ISA doesn't tell the microarchitect 5 how to instantiate the instructions in the 6 microarchitecture?</p> <p>7 A So by instantiate an instruction, you mean 8 realize and implement it in your question?</p> <p>9 Q Correct.</p> <p>10 A Okay. There is -- there is leeway there, but 11 there is also guidance. Since we're talking in general, 12 I will use x86 as my example because that's the one I 13 know the best.</p> <p>14 When you do as I did, add a new -- a certain 15 set of new instructions to the architecture, you may also 16 inject a whole new set of registers as well.</p> <p>17 When you do that -- that's for performance 18 reasons. You only put the instructions in because you 19 hope it's going to boost performance.</p> <p>20 But once you've done that, you have to supply 21 it with registers. And once you've done that, if you 22 take a context swap, the operating system intervenes and 23 says, "Okay. I'm going to put you down and pick 24 something else up." Those registers have to be saved.</p> <p>25 And it didn't use to be part of the context</p>

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<p style="text-align: right;">Page 158</p> <p>1 sense, get some real feedback. If there's problems, you 2 can still address it before you have a full commercial 3 launch. 4 A Ideally that's what would happen, yeah. 5 Q And it's the microarchitectures -- right? -- 6 that come up with these millions of tests that they run 7 on their devices and their cores before they would take 8 it to market; right? 9 A In my experience, that's not a good idea. It's 10 really hard to have a designer who stays up nights and 11 weekends and doesn't see their kid's birthday trying to 12 give birth to something and then have them attack it, 13 which is what -- 14 Q They can't see their own faults? 15 A They just can't see. Exactly. I mean, there's 16 a common -- there's a common mode -- we call it a common 17 mode error where the same thing that you stuck in there 18 is going to allow you to miss it as a fault because you 19 thought it was right in the first place. 20 In my personal opinion, it's a much better idea 21 to have a set of validators that it's their only job, is 22 to attack your baby and see if there's anything wrong 23 with it because it's far better if they find it than 24 someone else. 25 And, by the way, the ratio of designers to</p>	<p style="text-align: right;">Page 160</p> <p>1 -- two of the wires on the chip are too close together. 2 Q Whether they can build it; right? 3 A Yeah, design rules. 4 Q Yeah, yeah, yeah. 5 A They do design rule checking. And they'll -- 6 they'll also give you back some indicators of, "Hey, you 7 said this should run at -- you should get good yield at 3 8 gigahertz, but the testing I'm doing on it, in my initial 9 checks, say you're only going to get the 2.1 gigahertz. 10 Is that okay with you?" And you'd better track that down 11 if that's -- if that's -- 12 Q If it's important? 13 A -- if it's, in fact, important to you. 14 Q Yeah. And so the ACK test, my [REDACTED] 15 [REDACTED] 16 A Uh-huh. 17 Q [REDACTED] 18 But it is definitely a part of the process, you 19 know, of testing whether -- you know, whether your 20 ultimate CPU is going to work? 21 And by that, I mean, the ACK, though, is 22 focused on whether or not you're complying with the 23 architecture roles; fair? 24 A I think that's the intent of it. 25 Q And would you agree with me that that's one</p>
<p style="text-align: right;">Page 159</p> <p>1 validators has gone from ten to one -- did I say it 2 right? -- yeah, ten designers to one validator back in 3 the '80s; to today, it's about two validators per 4 designer. There are more people testing than there are 5 designing because the problem is so difficult and scales 6 so poorly. 7 Q Interesting. It feels a little bit like, you 8 know, when I read a brief 20 times before I file it and 9 then -- and then somebody else takes a look at it and 10 sees the typo; right? 11 A Yep. 12 Q I get that. And this is done, though, 13 internally by the companies that are making these 14 devices; right? 15 A The presilicon testing is normally done by 16 the -- some group that's associated with the design team. 17 Q Right. And you have, like, the TSMCs of the 18 world. I mean they're going to do even further 19 testing -- right? -- before you go full-scale silicon? 20 A Yeah, although their testing is of a 21 specialized nature. 22 Q Right. 23 A They don't really know what your chip is 24 supposed to do, but they can tell by looking at the 25 database you handed them whether the -- two of the routes</p>	<p style="text-align: right;">Page 161</p> <p>1 small piece of, really, the full testing that needs to be 2 done on these SoCs, you know, before you -- even before 3 you tapeout? 4 A Oh, of the SoC, yeah -- well, I agree with that 5 to the extent that the CPUs are just one part. I won't 6 say small because they're pretty important, but they're 7 only one part of what goes onto that SoC. 8 And the ACK is only going to help you, at least 9 on first order, with the health of those processors. 10 They're not going to tell you if there's something wrong 11 with the wrapper that you stuck on the USB 3, for 12 example. 13 Q Because the ACK is only focused on the CPU? 14 A Yes. 15 Q And there's lots of other tests that are also 16 run on the CPU separate and apart from the ACK? 17 A I would hope so. But, you know, they're hard 18 to write. They're expensive. They're hard to maintain. 19 I mean, it's a -- it's a nontrivial investment by the 20 company to create any other tests and then maintain them 21 then on. But I would hope they do it. 22 Q You'd be surprised -- wouldn't you? -- if a 23 company like Qualcomm is not running a significant amount 24 of tests on its CPU separate and apart from the ACK 25 tests?</p>

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<p style="text-align: right;">Page 162</p> <p>1 A It would be a little bit surprising. It</p> <p>2 wouldn't surprise me if a start-up tried to live with</p> <p>3 just the ACK because, as I said, this is expensive. And</p> <p>4 they may not be able to afford to do better than that.</p> <p>5 And they're just going to have to try and hope for the</p> <p>6 best.</p> <p>7 MS. NYARADY: All right. I think we're</p> <p>8 probably at a good point for lunch, if that reduced</p> <p>9 instruction set computer sense.</p> <p>10 THE WITNESS: Uh-huh.</p> <p>11 THE VIDEOGRAPHER: The time is 1:10 p.m. Off</p> <p>12 record.</p> <p>13 (A lunch recess was taken.)</p> <p>14 THE VIDEOGRAPHER: The time is 2:03 p.m. We're</p> <p>15 back on record.</p> <p>16 BY MS. NYARADY:</p> <p>17 Q Earlier, I had asked you a question and then I</p> <p>18 think we got turned around and went to another question</p> <p>19 and then I realized I never got -- don't think I ever got</p> <p>20 a full answer.</p> <p>21 So let me ask -- let me ask this: Does the ISA</p> <p>22 provide information to the microarchitect as to how to</p> <p>23 perform fetching?</p> <p>24 A I actually don't remember you asking that</p> <p>25 earlier. But I believe you if you said you did.</p>	<p style="text-align: right;">Page 164</p> <p>1 self-modifying code, there are certain things that you</p> <p>2 absolutely must do in terms of where you cache the</p> <p>3 instructions and what you do if the code gets modified</p> <p>4 that's already been cached.</p> <p>5 It gets complicated fast, but if you don't</p> <p>6 allow it at all, this issue goes away. And so it's not</p> <p>7 really a guardrail thing. It's more, like, if you -- if</p> <p>8 you have to have this feature, then you have to do</p> <p>9 certain things.</p> <p>10 Q And you're not sure either way whether ISA has</p> <p>11 this feature?</p> <p>12 A Yeah, I am not. I don't remember.</p> <p>13 MS. NYARADY: I am going to hand you what was</p> <p>14 previously marked as QX242 at Dr. Chen's deposition.</p> <p>15 And just represent to you this is an excerpt of</p> <p>16 the Arm ARM; specifically if you look at the bottom of</p> <p>17 the first page, the front page, which is Bates-numbered</p> <p>18 ARM_01324149, it is Version 8.7, G.b.</p> <p>19 (Previously marked Exhibit QX242.)</p> <p>20 BY MS. NYARADY:</p> <p>21 Q And it is the first several pages and then the</p> <p>22 -- the contents, table of contents for the Arm ARM.</p> <p>23 As you know, this document is quite large, so</p> <p>24 we didn't bring the entire document. We do have it</p> <p>25 electronically. If you need to look at any of it, please</p>
<p style="text-align: right;">Page 163</p> <p>1 It can. In general, an architecture can do</p> <p>2 that.</p> <p>3 Q How so?</p> <p>4 A For instance, there are some architectures that</p> <p>5 don't allow self-modifying code. Do you know what that</p> <p>6 is or should I elaborate?</p> <p>7 Q I don't think you need to elaborate on that.</p> <p>8 Does the Arm ISA provide microarchitects</p> <p>9 information on how to perform fetching?</p> <p>10 A I'm actually not sure whether they allow</p> <p>11 self-modifying code or not, so I can't answer.</p> <p>12 The point if you don't allow self-modifying</p> <p>13 code or if you do, it gives you -- that tells you what</p> <p>14 you have to do in terms of caching those instructions in</p> <p>15 the fetch part of the operation because if they can be</p> <p>16 changed, you have to treat them in a slightly different</p> <p>17 way than if they cannot be.</p> <p>18 But since I don't -- I just don't happen to</p> <p>19 know what Arm's rule is for that.</p> <p>20 Q Whether or not it allows self-modifying code,</p> <p>21 would this be another example of where there are</p> <p>22 guardrails of things you can do versus giving specific</p> <p>23 instructions about how to code for fetching?</p> <p>24 A Well, it's sort of a guardrail thing, but it's</p> <p>25 -- it's -- I view this one more as if they allow</p>	<p style="text-align: right;">Page 165</p> <p>1 let me know. But, really, my focus -- I'm hoping you can</p> <p>2 answer these questions just based on the pages I gave</p> <p>3 you.</p> <p>4 If you look at your report, which we've marked</p> <p>5 as QX248, your opening report, and if you turn to -- the</p> <p>6 section starts on Page 26. You should feel free to look</p> <p>7 at anything you need.</p> <p>8 But I wanted to draw your attention to Page 28</p> <p>9 and 29 because my questions are simple with respect to</p> <p>10 this exhibit.</p> <p>11 I just want to confirm that when you're citing</p> <p>12 to the Arm ARM in your report for certain things -- so,</p> <p>13 for example, on Page 28 and Page 29, you have images</p> <p>14 of -- it looks like just maybe a screenshot of the Arm</p> <p>15 ARM.</p> <p>16 I just want to confirm that this is QX242.</p> <p>17 That is the version of the Arm ARM that you have looked</p> <p>18 at and relied on for the purposes of your opinions in</p> <p>19 that opening report; correct?</p> <p>20 A Yeah, it appears to be the same one.</p> <p>21 Q Okay. Was there any other version of the Arm</p> <p>22 ARM that you relied on for purposes of your opinions? I</p> <p>23 mean, for example, there's parts -- I want to say even</p> <p>24 the page previously -- you talk about the latest version</p> <p>25 being a V9. You mentioned that earlier today.</p>

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<p style="text-align: right;">Page 166</p> <p>1 Did you do the same type of analysis with --</p> <p>2 with v9 or with any other version of the Arm ARM?</p> <p>3 A No. Where I mentioned v9 is just along the</p> <p>4 lines of the Nuvia team knew that that was under</p> <p>5 development and chose to stick with V8.7 because</p> <p>6 Version 9 wasn't ready yet. And it would have -- it</p> <p>7 could have potentially impacted their schedule and they</p> <p>8 didn't want to do that.</p> <p>9 Q And Nuvia actually never got a license to</p> <p>10 v9; right?</p> <p>11 A Not as far as I know.</p> <p>12 Q Okay. So, again, just to confirm, this was the</p> <p>13 version that has the starting Bates numbers that I marked</p> <p>14 as QX242, so the V8.7 G.b, that was the version of the</p> <p>15 Arm ARM that you used in your analysis in forming your</p> <p>16 opinions; correct?</p> <p>17 A Yeah, that's the -- Version 8.7 is the one that</p> <p>18 I assumed in all of the work that I did.</p> <p>19 Q And I don't know the significance of it, but it</p> <p>20 says Capital G, lowercase b.</p> <p>21 That's the name of the version; right?</p> <p>22 A I never called it that, so I don't know</p> <p>23 offhand. I'm trying to figure it out.</p> <p>24 Q If you look at Page 20 of your report,</p> <p>25 Paragraph 60, you actually do call it that. That's why</p>	<p style="text-align: right;">Page 168</p> <p>1 for. If you go to Paragraph 167 of your report, it's on</p> <p>2 Page 88, there is where you're talking about Dr. Chen</p> <p>3 finding features from the Arm 2020 architecture</p> <p>4 extensions.</p> <p>5 And then the Bates number in your report</p> <p>6 matches that of QX244; correct?</p> <p>7 A Hang on a second. I'm not tracking your</p> <p>8 question. Sorry, point me to where --</p> <p>9 Q Sure. You're at Paragraph 167?</p> <p>10 A Yes.</p> <p>11 Q Okay. About three lines down, there's a</p> <p>12 sentence that starts, "For example." And then it says,</p> <p>13 [REDACTED]</p> <p>14 [REDACTED] There's a parenthetical with a Bates</p> <p>15 number. And then it says, after the parenthetical,</p> <p>16 "which is marked as Arm confidential."</p> <p>17 Does that Bates number match QX244?</p> <p>18 A The Bates number being ARM_00099622?</p> <p>19 Q Correct.</p> <p>20 A It does match, yes.</p> <p>21 Q Is this the --</p> <p>22 Is QX244 the [REDACTED]</p> <p>23 document that you relied on for your opinions relating to</p> <p>24 the extensions you allege are found in the Qualcomm</p> <p>25 custom cores?</p>
<p style="text-align: right;">Page 167</p> <p>1 I'm trying to match that up.</p> <p>2 A Oh, with the G? I see.</p> <p>3 Q Yeah. And, again, this is, you know, more</p> <p>4 clerical in the sense that I'm just trying to confirm</p> <p>5 that this is the version of the Arm ARM that you used in</p> <p>6 forming your opinions.</p> <p>7 A I think it is, yes.</p> <p>8 MS. NYARADY: Okay. Similarly, I want to show</p> <p>9 you a document that was previously marked at Dr. Chen's</p> <p>10 deposition as QX244. This is the Arm 2020 architecture</p> <p>11 extensions. The Bates numbers from this case are</p> <p>12 ARM_00099622 through 657.</p> <p>13 (Previously marked Exhibit QX244.)</p> <p>14 BY MS. NYARADY:</p> <p>15 Q And if you look on Page 29, I believe, of your</p> <p>16 report, you talk about -- actually, maybe you don't cite</p> <p>17 to it there. In Paragraph 61, you do talk about updates</p> <p>18 to the Arm ARM periodically.</p> <p>19 And then later in the report, you talk about</p> <p>20 the extension that Dr. Chen identified a comment of which</p> <p>21 being in the source code for the Qualcomm custom cores.</p> <p>22 Do you recognize this document, QX244?</p> <p>23 A I'm sure I've seen it before. I don't</p> <p>24 immediately recognize it. I know what it is.</p> <p>25 Q Okay. And I did find the cite I was looking</p>	<p style="text-align: right;">Page 169</p> <p>1 A I think so.</p> <p>2 Q And just to be clear, this is a -- these</p> <p>3 extensions, this is a confidential document; right?</p> <p>4 A Uh-huh.</p> <p>5 Q And, actually, [REDACTED]</p> <p>6 [REDACTED]</p> <p>7 [REDACTED]</p> <p>8 [REDACTED]</p> <p>9 A Yes.</p> <p>10 Q Okay. And then, actually, [REDACTED] And</p> <p>11 [REDACTED]</p> <p>12 then it cites to some other documents.</p> <p>13 Do you see that?</p> <p>14 A Yes.</p> <p>15 Q And [REDACTED]</p> <p>16 [REDACTED]</p> <p>17 And that's the Arm ARM that we've been talking</p> <p>18 about; right?</p> <p>19 A Yes.</p> <p>20 Q So this document, if I understand it correctly</p> <p>21 -- and please feel free to look at the cover as well --</p> <p>22 it says that [REDACTED]</p> <p>23 [REDACTED]</p> <p>24 And my understanding is that these are</p> <p>25 architecture specifications that Arm is actively working</p>

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1 it is Bates number QCARM_0315570 through 83.
2 And for completeness, I am also going to mark
3 Annex 1, since you cited in your report, the original
4 Annex 1 for the Nuvia/Arm ALA, which is dated
5 September 27th, 2015. I've marked it as QX251. And it
6 is Bates number QCARM_03393010 through 325.
7 (Exhibits QX249, QX250, & QX251
8 marked.)
9 BY MS. NYARADY:
10 Q In your opening report -- if you'd like to look
11 at it, it's at Paragraph 74 -- but you say that,
12 obviously, you're not an expert on -- and you've already
13 said you're not a legal expert or an expert on licensing.
14 But you say that you understand that the
15 Arm/NOVIA ALA agreement gave Nuvia the right to design
16 and market a custom Arm-compliant core under that
17 agreement.
18 Where did you gain that understanding? Is that
19 your understanding from reading the agreement, or were
20 you instructed by counsel or something else?
21 A I was basically told that that was the
22 situation. And then I read the documents in question and
23 they looked like they were in agreement to me.
24 Q Okay. In Paragraph 75 of your report, the
25 heading just above Paragraph 75 on Page 36 says,

The image shows a series of 20 horizontal bars, each representing a value on a scale from 0 to 100. The bars are arranged in a grid-like pattern with labels on the left and right sides. The labels on the left are '1', '2', '3', '4', '5', '6', '7', '8', '9', '10', '11', '12', '13', '14', '15', '16', '17', '18', '19', and '20'. The labels on the right are '0', '10', '20', '30', '40', '50', '60', '70', '80', '90', and '100'. The bars are of varying lengths, with the longest bar (labeled '1') reaching approximately 95% and the shortest bar (labeled '19') reaching approximately 10%.

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1 [REDACTED]
 2 [REDACTED]
 3 [REDACTED]
 4 [REDACTED]
 5 [REDACTED]
 6 [REDACTED]
 7 [REDACTED]
 8 [REDACTED]
 9 [REDACTED]
 10 [REDACTED]
 11 [REDACTED]
 12 [REDACTED]
 13 [REDACTED]
 14 [REDACTED]
 15 [REDACTED]
 16 [REDACTED]
 17 BY MS. NYARADY:
 18 Q Okay. I believe you said earlier you had not
 19 reviewed the Qualcomm ALA; is that right?
 20 A I think that's true. I don't think I've ever
 21 seen it.
 22 Q So you don't have an opinion -- I don't think I
 23 saw it in the report, but for completeness, I want to
 24 ask: You don't have an opinion -- do you? -- or you're
 25 not planning on offering an opinion with respect to how

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1 if at all, [REDACTED]
 2 [REDACTED]
 3 [REDACTED]
 4 Is that accurate?
 5 A Not in a legal sense. I would not offer an
 6 opinion like that. In a technical sense, I know that
 7 they have the ACK, for example. I know that Qualcomm had
 8 access to Arm engineers because I saw some of the emails
 9 and so on.
 10 So -- and that's what I would expect with
 11 somebody with an ALA license. Those are the things that
 12 you would get with that.
 13 Q And -- okay.
 14 And specifically with respect to the [REDACTED]
 15 [REDACTED] would you be offering any opinion as
 16 to whether the [REDACTED]
 17 [REDACTED]
 18 [REDACTED]
 19 A I hope not. I do not intend to do that.
 20 Q Okay. You are not planning -- are you? -- to
 21 offer any opinion as to whether or not the engineering
 22 work performed at Qualcomm post-acquisition, whether it
 23 is properly -- and by "properly," I mean legally -- under
 24 the Qualcomm ALA, are you?
 25 A No. That sounds like a legal thing to me.

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1 Q Right.
 2 A And that's not my part.
 3 Q What I'm -- what I mean to say is that whether
 4 or not the Qualcomm ALA gives Qualcomm the right to do
 5 whatever work it did post-acquisition.
 6 That's not -- you haven't been asked to do that
 7 assessment, have you?
 8 A I did -- I did consider the question of what --
 9 if Qualcomm were to use the part -- Nuvia's design,
 10 which, I believe, does qualify as derivative of [REDACTED]
 11 [REDACTED] under Nuvia's rules, if they were to use that
 12 in other products, I believe that derivative aspect
 13 carries through. But, for example -- so that's one
 14 extreme.
 15 The other extreme is to the extent that
 16 Qualcomm is doing new designs that weren't given to them
 17 in any way from Nuvia, I have nothing to say about that.
 18 I understand they have an ALA. And it would make sense
 19 to go and do whatever they need to do.
 20 Q But there -- the question I'm asking -- and I
 21 appreciate that. That's helpful for the two, I guess,
 22 ends of the spectrum.
 23 A Uh-huh.
 24 Q The question I'm asking, perhaps is maybe more
 25 in the middle, which is: I understand you have opinions

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1 as to [REDACTED]
 2 [REDACTED]. Understood.
 3 You, though, are not going to opine -- are you?
 4 -- as to whether or not Qualcomm, as a corporation, is
 5 allowed to do certain work post-acquisition under its own
 6 ALA, are you?
 7 A No. I don't think I would be able to do that
 8 if I tried because I have not seen the ALAs.
 9 Q Okay. And you talk about Qualcomm -- I want to
 10 make sure I get your words right.
 11 You mentioned earlier in your last answer
 12 Qualcomm doing new designs that weren't given to them in
 13 any way from Nuvia; right?
 14 You don't dispute -- do you? -- or yeah, you
 15 don't dispute that Qualcomm could have hired all of the
 16 Nuvia engineers and had those Nuvia engineers do a clean
 17 sheet project to build new custom cores, do you?
 18 A If Qualcomm was doing a clean sheet new custom
 19 core, I don't care who works on it. I mean, I don't
 20 think it's relevant.
 21 Q Okay. And so the fact that it would be Nuvia
 22 engineers that come over, become Qualcomm employees and
 23 do that, you would not say that somehow reduced
 24 instruction set computer the work, then, done at Qualcomm
 25 derivative?

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<p style="text-align: right;">Page 186</p> <p>[REDACTED]</p> <p>[REDACTED]</p> <p>3 Q And I don't see that opinion anywhere in your</p> <p>4 report. I understand what you're saying. You're</p> <p>5 pointing to the section of the definitions -- actually,</p> <p>6 you're pointing to a section that says, [REDACTED]</p> <p>[REDACTED]</p> <p>8 And now you're saying that the [REDACTED]</p> <p>[REDACTED] may also be, I guess, in the</p> <p>10 Qualcomm cores or you're hypothesizing that it could be,</p> <p>11 if I'm following you.</p> <p>12 But I don't see -- when you get to the analysis</p> <p>13 of the Qualcomm cores, I don't ever see you saying that</p> <p>14 you have found [REDACTED] in the Qualcomm cores. I</p> <p>15 see an analysis of derivatives.</p> <p>16 A Okay. But that's partly because I see them as</p> <p>17 closely related things, if not synonymous.</p> <p>18 Q Well, they're definitely not synonymous; right?</p> <p>[REDACTED]</p> <p>[REDACTED]</p> <p>[REDACTED]</p> <p>[REDACTED]</p> <p>23 A I'm approaching it from a technical point of</p> <p>24 view. To me, that was a legal point of view. And I'm</p> <p>25 not going to dispute that.</p>	<p style="text-align: right;">Page 188</p> <p>1 it is the way it is because the architecture is the way</p> <p>2 it is. There's a link, sort of a conceptual abstract</p> <p>3 link, by which the architecture influences the decisions</p> <p>4 made at the microarchitecture level.</p> <p>5 An easy example was if they added a crypto</p> <p>6 instruction and you wanted to use their crypto scheme,</p> <p>7 then you have to -- you have to put that in there.</p> <p>8 Q And a couple of follow-ups on that. One is I</p> <p>9 mean, I don't see anywhere in the report where you say</p> <p>10 that those crypto exceptions are in the Qualcomm cores.</p> <p>11 Do you know whether you did that analysis or</p> <p>12 whether it's in the report?</p> <p>[REDACTED]</p> <p>[REDACTED]</p> <p>[REDACTED]</p> <p>[REDACTED]</p> <p>[REDACTED]</p> <p>[REDACTED]</p> <p>20 Q Okay. And the definition that you just</p> <p>21 provided of derivative, that is nowhere in your</p> <p>22 report; correct?</p> <p>23 A The -- so Paragraph 85 of my opening report, I</p> <p>24 didn't literally say, "This is how I define derivative."</p> <p>25 But that's more of a function of the way I think as</p>
<p style="text-align: right;">Page 187</p> <p>1 But from a technical point of view, I'm having</p> <p>2 a hard time distinguishing something that would be in the</p> <p>3 chip that I would not call Arm Technology but would call</p> <p>4 a derivative of it.</p> <p>5 I'm not saying it can't happen. I'm just</p> <p>6 saying that's my reaction to it, is I feel like they're</p> <p>7 synonymous from a technical level.</p> <p>8 Q Can you find me anywhere in your report where</p> <p>9 you have an opinion where there is [REDACTED] -- I'm</p> <p>10 not trying to be difficult. I need to be very clear as</p> <p>11 to what you're going to testify to at trial. And if -- I</p> <p>12 don't see anywhere in the report where you say there is</p> <p>13 [REDACTED] in the Qualcomm cores.</p> <p>14 So can you -- you know, we'll have a whole</p> <p>15 conversation about derivatives. That's fine.</p> <p>16 But can you show me where you disclose that</p> <p>17 opinion, if at all, in this report?</p> <p>18 A Yeah, I mean, I can search the whole report.</p> <p>19 But I won't be surprised if I can't find that and the</p> <p>20 reason is because, in my mind, they're the same.</p> <p>21 Yes, in general, I think they're so closely</p> <p>22 related that you can -- that they mean the same thing.</p> <p>23 Q So if they mean the same thing, what is your</p> <p>24 definition of "derivative"?</p> <p>25 A On a technical level, I think derivative means</p>	<p style="text-align: right;">Page 189</p> <p>1 opposed to, you know, this is -- I'm trying to explain</p> <p>2 it. I tried to explain it in Paragraph 85 the same way I</p> <p>3 just did with you, which is, "This is how I think about</p> <p>4 it."</p> <p>5 Q I see. Okay. Okay.</p> <p>[REDACTED]</p> <p>[REDACTED]</p> <p>[REDACTED]</p> <p>[REDACTED]</p> <p>[REDACTED]</p> <p>[REDACTED]</p> <p>13 Q Now, if that core is then put into an SoC, is</p> <p>14 it your opinion that the entire SoC is a derivative as</p> <p>15 well?</p> <p>16 A I don't remember opining on that. Do you know</p> <p>17 that there's somewhere in here that you can point me to?</p> <p>18 I can check.</p> <p>19 Q I actually don't remember.</p> <p>20 A I pretty much stuck to the core and didn't</p> <p>21 really worry too much about the SoC, so I'm going to be a</p> <p>22 little surprised if there's such a thing.</p> <p>23 Q But what do you -- what do you think as you sit</p> <p>24 here? Would it be -- would the SoC then be a derivative</p> <p>25 too?</p>

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1 Q Did you --

5 MR. MUINO: Objection. Form.

9 BY MS. NYARADY:

10 Q Okay. Fair point.

15 MR. MUINO: Objection. Form.

16 THE WITNESS: Well, it feels like we're having
17 a legal argument, which I don't -- I don't have expertise
18 for that.

19 BY MS. NYARADY:

20 Q Okay. That's fine. I mean, if you don't know,
21 that's fine. If it's --

22 A Okay.

23 Q -- a legal question.

24 A I'm not reading it that way, so.

4 Q So let me ask you a question --

5 Let me ask you this question: Is the Arm ARM
6 that's on the internet confidential information?

7 A I don't know the answer to that. I think
8 that's a legal issue. I actually don't understand the
9 relationship of how they license it to you and support
10 it. Otherwise, they put some version of it on the
11 internet.

12 Q But in applying the definition that you just
13 did, that you said is your understanding of what
14 confidential information is, the version of the Arm ARM
15 that's on the internet would not satisfy that
16 definition; correct?

17 MR. MUINO: Objection. Form.

18 THE WITNESS: It wouldn't seem to me. But it's
19 kind of irrelevant for the opinions that I offered.

20 To me, where it's relevant, potentially, is the
21 legal aspects, which you guys get to argue about.

22 BY MS. NYARADY:

23 Q Okay. Did you receive --

24 In formulating your opinions and relying on the
25 definition of [REDACTED] or [REDACTED]

1 or "██████" did you receive any instructions from
2 counsel as to -- or anyone -- as to how you should
3 interpret those terms?

4 Or did you do your technical analysis with your
5 understanding of those terms?

6 A Well, I definitely did it with my understanding
7 of the terms. But they were partly informed by
8 discussions with other people, including counsel, but
9 also including, for example, Richard Grisenthwaite and
10 having read his depo.

11 I believe related topics came up in that depo
12 that he addressed.

13 Q Okay. What -- what discussion --

14 What did counsel say that informed your
15 understanding of the terms?

16 MR. MUINO: And you can -- sorry -- you can
17 answer that question to the extent that communications
18 with counsel informed your opinions.

19 THE WITNESS: I remember having discussions
20 with counsel where I was trying to find the -- if there
21 was a boundary or a border between the ramifications of
22 thinking about it as a legal issue and thinking about it
23 as a technical issue. I wanted to see if there was a
24 fence that I could rely on. So that's the discussion --
25 that's what I mean by when talking to counsel about it.

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<p style="text-align: right;">Page 198</p> <p>1 And the other thing I remember from that</p> <p>2 discussion was the reenforcement of my need to remind</p> <p>3 myself I'm not a lawyer all the time and not to approach</p> <p>4 this as a, "Oh, well, you know, a reasonable</p> <p>5 interpretation of this would be blah," because that's --</p> <p>6 that's legal.</p> <p>7 And there is -- I don't know what a reasonable</p> <p>8 interpretation would be at that level.</p> <p>9 BY MS. NYARADY:</p> <p>10 Q So when you were trying to -- when you were</p> <p>11 trying to figure out what you called a border, you know,</p> <p>12 or fence to rely on about the legal issue versus the</p> <p>13 technical issue, what did counsel tell you about that?</p> <p>14 MR. MUINO: And, again, you can respond to that</p> <p>15 question to the extent that any communication with</p> <p>16 counsel was something you relied upon for your opinions.</p> <p>17 THE WITNESS: Yeah, I didn't -- I don't feel</p> <p>18 like I'm relying on what counsel told me in that</p> <p>19 conversation.</p> <p>20 It's more like I felt like I was -- the</p> <p>21 contribution I was trying to make was what is the</p> <p>22 connection between what's in, for example, the Arm ARM or</p> <p>23 the [REDACTED] and what it contributes or what its connections</p> <p>24 are inside the actual final product, including the</p> <p>25 microarchitecture.</p>	<p style="text-align: right;">Page 200</p> <p>1 MR. MUINO: Again, you can respond to that to</p> <p>2 the extent that communications with counsel did, in fact,</p> <p>3 inform your opinions.</p> <p>4 MS. NYARADY: Well, he's testified that they</p> <p>5 did. It's an improper instruction.</p> <p>6 MR. MUINO: No, it's not.</p> <p>7 MS. NYARADY: I'm asking about your testimony.</p> <p>8 THE WITNESS: I didn't -- I did not mean to</p> <p>9 give the impression that I'm agreeing that counsel</p> <p>10 informed my opinions. I'm saying we had discussions when</p> <p>11 I was thinking about these things, especially earlier on.</p> <p>12 And I was trying to find the technical path that would</p> <p>13 belong to me, that I would have to focus on.</p> <p>14 And it was in that sense that counsel would</p> <p>15 say, you know, "This argument constitutes a legal issue"</p> <p>16 or "That argument does not and that's where you belong,</p> <p>17 it would be over here."</p> <p>18 It wasn't -- it wasn't specific about, "Here's</p> <p>19 the answer we want you to remember." It wasn't -- it</p> <p>20 wasn't at that level.</p> <p>21 BY MS. NYARADY:</p> <p>22 Q And it wasn't about the definition of any of</p> <p>23 the words that we're talking about, [REDACTED]</p> <p>[REDACTED]</p>
<p style="text-align: right;">Page 199</p> <p>1 I was concentrating on that and sort of</p> <p>2 applying it against my background of designing things and</p> <p>3 saying, "What's the sequence of events? And what do you</p> <p>4 do first?" I was even -- I remember being asked, "Can</p> <p>5 you design a chip and, at the last minute, make it</p> <p>6 compatible with some architecture?" Issues like that.</p> <p>7 And I'd say, "No, that's not how those things</p> <p>8 work." Anyways, I was always approaching it from the</p> <p>9 technical point of view and trying to, sort of, add value</p> <p>10 at that level and not trying to define it, per se.</p> <p>11 BY MS. NYARADY:</p> <p>12 Q Okay. Earlier, you said -- I was asking about</p> <p>13 your understanding of the terms [REDACTED]</p> <p>[REDACTED]</p> <p>15 And I asked, "Did you receive any instructions</p> <p>16 from counsel or anyone with respect to those terms?"</p> <p>17 In your answer, you said, "They were partly</p> <p>18 informed by discussions with other people, including</p> <p>19 counsel."</p> <p>20 So what did you mean by that?</p> <p>21 A I literally meant I know that I had discussions</p> <p>22 in which that topic came up, discussions with counsel</p> <p>23 when -- at which that topic came up.</p> <p>24 Q And how were your definitions that you applied</p> <p>25 in rendering your opinions informed by counsel?</p>	<p style="text-align: right;">Page 201</p> <p>1 A No. Well, as you saw, I didn't try to define</p> <p>2 derivative in its technical sense. I just -- I'm not</p> <p>3 even -- I'm not sure that's a good exercise because I</p> <p>4 think that leads directly into legal issues that I can't</p> <p>5 help with.</p> <p>6 So, instead, I tried to say, "These are the --</p> <p>7 this is the way I look at this stuff that leads me to the</p> <p>8 conclusions that I stated in various places that the</p> <p>9 architecture affects the microarchitecture in some</p> <p>10 important ways."</p> <p>11 Q And under your definition or how you think</p> <p>12 about what a derivative is, that's a derivative?</p> <p>13 A Yes.</p> <p>14 Q Okay. What does it mean to embody certain</p> <p>15 technology or information? Is that different -- do you</p> <p>16 look at that as different than derivative?</p> <p>17 A I believe I could come up with cases where one</p> <p>18 word fits better than the other one. But I think they're</p> <p>19 both in the same general category.</p> <p>20 Q Okay. Did you use a definition --</p> <p>21 In forming your opinions, did you use a</p> <p>22 definition of "recast"?</p> <p>23 A That's not a word I use very often, so no, I</p> <p>24 don't think I needed that one.</p> <p>25 Q Is that a term of art in your field?</p>

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<p style="text-align: right;">Page 202</p> <p>1 A I certainly have not run into it very often, if 2 at all. 3 Q In forming your opinions, did you use a 4 definition for the word [REDACTED] 5 A I don't think of it as using a definition. I 6 think of it as taking the English word and my general 7 understanding of it and finding if there's an analogue in 8 the design process for which that word looks pretty 9 appropriate. 10 And for both [REDACTED], that mapping 11 feels pretty natural, so I didn't try to come up with 12 definitions for those. I just used them the way I 13 understood them. 14 Q And just to make sure I understand, so the 15 mapping that you're talking about is using the Arm 16 architecture or the Arm architecture influencing the 17 core? 18 A [REDACTED] in general because I would 19 include the ACK in that. 20 Q Okay. So the [REDACTED] as you define it, 21 influence -- or -- 22 A Or as I think of it. 23 Q Okay. Influencing the core, that mapping, in 24 your mind, satisfies the general [REDACTED] [REDACTED]</p>	<p style="text-align: right;">Page 204</p> <p>1 property blocks with an interconnect in the middle. And 2 that interconnect has a certain set of protocols and 3 standards that it embodies. 4 In order to get onto that network and get it 5 across to where you're going, you either have to speak 6 its native language or you have to convert your native 7 language to it. 8 And that thing that does the conversion, one of 9 the words they might use for that is [REDACTED] And, 10 again, the wrapper thing is one of the things that has to 11 do, commonly, is that conversion. 12 Q Okay. Thank you. I don't think I asked you 13 the same question about transform. 14 Is [REDACTED] a term of art in your industry? 15 A Yeah, very much so. 16 Q And what does that mean? 17 A Usually, it means convert something from one 18 format to another format. 19 Q Can you give me an example. 20 A The only example that's coming immediately to 21 mind is not very relevant to this case. There are -- 22 well, I'll tell it to you anyway. 23 There are transforms. There's a thing called a 24 fast fourier transform. It's all software. I mean, you 25 can put hardware on it, but it's extremely -- that's how</p>
<p style="text-align: right;">Page 203</p> <p>1 A Well, more precisely, I would say there are -- 2 there are examples for which the -- some of the [REDACTED] [REDACTED] manifests in the design of the machine in such 4 a way that use of the word "[REDACTED]" or [REDACTED] 5 would be appropriate to describe that motion. 6 Q Okay. And is the same thing through for 7 [REDACTED] 8 A Yes, I think so. 9 Q Okay. Is the word "[REDACTED]" a term of art in 10 your field? 11 A That one is, yes. 12 Q What does it mean? 13 A It means something that's -- something has to 14 be modified because of some larger goal. For example, 15 people will speak of adapting the intellectual property 16 blocks on an SoC by putting that wrapper around it that 17 we talked about earlier. 18 And that would be -- they would call that 19 adapting it for their SoC. 20 Q And what is -- what is it they're doing -- what 21 are they [REDACTED] it for? 22 A You mean the motivation or? 23 Q Yeah, I guess I'm just not fully following your 24 example. 25 A Okay. So many SoCs have lots of intellectual</p>	<p style="text-align: right;">Page 205</p> <p>1 radar works. That's how they do it. 2 And it transforms information from the time 3 domain to the frequency domain. So instead of having to 4 count cycles to see, you know, what the various 5 frequencies are over here, instead you just do the 6 transform and they just stick out. They just pop out. 7 The military loves the FFT. They use it constantly. 8 And so everyone in -- all practitioners in the 9 art would know what transform means and why you're using 10 the word transform. In this context, it's less clear. 11 Q Okay. Are you aware that Mr. Grisenthwaite 12 testified that [REDACTED] [REDACTED] 14 Are you aware of that? 15 A Yes. 16 Q And you disagree with him? 17 A I disagree -- so it was funny because I read 18 his deposition and I saw that he said that. And then I 19 talked to him after that. 20 And I specifically brought that up and said, [REDACTED] [REDACTED] [REDACTED] 24 And I expected him to say, "Oh, I see your 25 point. Yeah, we'll do that." But he didn't. He said,</p>

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1 "It's a matter of taste." It's a matter -- he said it's
2 not even a matter of technical taste. This an English
3 thing. And, of course, when a person in England tells
4 you they don't like your English, it's kind of awkward.
5 So anyway, I didn't push it very far. I just
6 took it as okay. Some people like certain words and some
7 people don't. I didn't see that we had any technical
8 disagreement.

9 Because, you know, after that, I did talk to
10 him about other things. What am I going to find in the
11 Arm ARM? Why do I need it so badly? You know, we talked
12 about a lot of stuff like that. We weren't -- we weren't
13 disagreeing on that, I don't think.

14 But we did -- we just have different tastes on
15 the English language.

16 MS. NYARADY: We've been going over an hour.
17 Do you want to take a break?

18 THE VIDEOGRAPHER: Time is 3:18 p.m. Off
19 record.

20 (Break held off the record.)

21 THE VIDEOGRAPHER: The time is 3:40 p.m. We're
22 back on record.

23 BY MS. NYARADY:

§ 87(2)(b) § 87(2)(b) § 87(2)(b)

1 chapter? And you keep looking until you find the right
2 spot.

3 Then you have to actually study what's there.

4 And it's very hard because it's easy to misinterpret it.

5 So I think the act of -- the mental act of reading it but
6 then figuring out what it means in terms of the
7 technology being applied, to me, that feels like
8 translate's a pretty good word for [REDACTED] It's
9 a pretty good word.

10 Q It sounds like the process you're describing,
11 it's not a literal [REDACTED]

12 Is that fair?

13 A Well, in the sense that people will say I've
14 translated German to French. Not really. Because in
15 that case, at least they're both languages. But in this
16 case, you're going from written words on a page to
17 transistors and functions and things.

18 And that's a -- you're doing a lot of
19 changeover.

20 Q How does --

21 That definition you just gave me of [REDACTED] n
22 how does that differ from [REDACTED] Because I think you
23 said [REDACTED] is converting, you know, one format to
24 another. You gave me an example.

25 What's the difference between [REDACTED] and

[illegible]

15 Q Is [REDACTED] a term of art in your field?

16 A Yes.

17 O What does it mean?

18 A In its -- as a term of general art in my field,
19 I think it means you take something that's in one form
20 and you put it in a different form.

21 But [REDACTED] is often used in a -- I don't
22 know the words. A setting where words matter. So, for
23 instance, you look in the spec. You find the right
24 place. You read what's written there. You figure out is
25 this the best solution to my problem or am I on the wrong

1 translate?

2 A I think a lot of times there isn't one, but to
3 the extent that there's one, perhaps it's in -- my
4 inclination would be I would use translate if I was
5 emphasizing the aspect of reading the thing and
6 understanding what's written there in its full, you know
7 -- with all of the details that it's implying.

8 I'm pretending this is the Arm ARM.

9 Q You're acting it out. I appreciate that.

10 A Yeah, I know; right? But [REDACTED] means, "Oh,
11 I know what this is and I know what that is and I'm going
12 to convert that into that via some means." So, you know,
13 to me, it's a subtle distinction, if any.

14 Q How about the word "[REDACTED]" Did you
15 apply definition of "[REDACTED]" in rendering your
16 opinions?

17 A As best as I recall, I did not initially do
18 that, but I'm pretty sure that Dr. Annavaram brought it
19 up. And so then I -- because I definitely remember the
20 subject came up because I think he said something -- he
21 used the word [REDACTED] -- oh, I think it was in the
22 context of Nuvia did something to the instruction fetch
23 part and added some bits.

24 And I think he was using that to say that's a
25 [REDACTED] of some sort. But that's the only context I

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<p style="text-align: right;">Page 210</p> <p>1 can remember right now.</p> <p>2 Q So you didn't focus on modification in</p> <p>3 rendering your initial opinions in your opening report?</p> <p>4 A I think that's fair. Because I don't -- I</p> <p>5 don't think it's a licensee's job to modify what Arm</p> <p>6 tells them. It's to implement it properly, first and</p> <p>7 foremost. And if they have to [REDACTED] something, they had</p> <p>8 better work it out with Arm first.</p> <p>9 Q What about [REDACTED] Did you apply a</p> <p>10 definition of compilation in rendering your opinions?</p> <p>11 A I don't recall doing that in that many terms</p> <p>12 because, to me, [REDACTED] means combining, collecting</p> <p>13 things and putting them into one set.</p> <p>14 And you can do that, of course. Sometimes you</p> <p>15 have to do that when you pick and choose options from</p> <p>16 Arm, and you pay for the ones you picked and you don't</p> <p>17 pay for the other ones.</p> <p>18 You can say, "I've [REDACTED] a list of the</p> <p>19 features I want from you." But I don't remember calling</p> <p>20 it out in those terms.</p> <p>21 Q And the thing you're describing about listing</p> <p>22 the features, they all already would be in the Arm</p> <p>23 ARM; right?</p> <p>24 A Yeah, I think. Yes. Because there's a</p> <p>25 separate process for asking them for things that aren't</p>	<p style="text-align: right;">Page 212</p> <p>1 core, would that be a derivative of [REDACTED]</p> <p>2 A I'm not aware of --</p> <p>3 MR. MUINO: Objection. Form.</p> <p>4 THE WITNESS: -- that Arm allows that. I</p> <p>5 thought they only gave [REDACTED]</p> <p>6 [REDACTED]</p> <p>7 [REDACTED]</p> <p>8 But you're kind of mixing the two. And I</p> <p>9 didn't know you were allowed.</p> <p>10 BY MS. NYARADY:</p> <p>11 Q Let's assume that Arm has allowed people to do</p> <p>12 that.</p> <p>13 A To take an existing core that Arm provided and</p> <p>14 did and let them modify it?</p> <p>15 Q Correct.</p> <p>16 In that scenario, would that be a derivative of</p> <p>17 [REDACTED] Again, assuming that that core is a</p> <p>18 [REDACTED]</p> <p>19 MR. MUINO: Objection. Form.</p> <p>20 THE WITNESS: So I haven't worked on forming an</p> <p>21 opinion on that subject. My knee-jerk reaction is yes,</p> <p>22 it would be.</p> <p>23 BY MS. NYARADY:</p> <p>24 [REDACTED]</p> <p>25 [REDACTED]</p>
<p style="text-align: right;">Page 211</p> <p>1 in there but you wish you were.</p> <p>2 Q I just meant when you were saying pulling --</p> <p>3 when you're talking about a [REDACTED] and pulling from</p> <p>4 things, is part of the reason that doesn't really fit</p> <p>5 because they're already in one place?</p> <p>6 A I think so, yeah. That's probably -- I mean,</p> <p>7 I'm trying to figure out why -- why doesn't spring to</p> <p>8 mind -- why doesn't that word spring to mind when I'm</p> <p>9 thinking of this.</p> <p>10 And it just doesn't because it's not -- it</p> <p>11 doesn't seem to fit what I -- what I perceived to be the</p> <p>12 right process for designing.</p> <p>13 Q Okay. And then [REDACTED] I think we</p> <p>14 talked about. You're not really rendering an opinion on</p> <p>15 that either. That seemed like a word you weren't quite</p> <p>16 sure what to make of it?</p> <p>17 A Yeah, I did not use that. Yeah, that's</p> <p>18 correct.</p> <p>19 Q Okay. Okay. So this came up a little bit when</p> <p>20 you were talking about modify.</p> <p>21 But if a licensee were to get, under the ALA,</p> <p>22 what would otherwise be an off-the-shelf core, so say</p> <p>23 they got a Cortex core, but it was under the ALA. It was</p> <p>24 actually listed in the Annex 1, you know, as an [REDACTED]</p> <p>25 [REDACTED] and Arm allowed the licensee to modify that</p>	<p style="text-align: right;">Page 213</p> <p>1 [REDACTED]</p> <p>2 [REDACTED]</p> <p>3 [REDACTED]</p> <p>4 [REDACTED]</p> <p>5 [REDACTED]</p> <p>6 [REDACTED]</p> <p>7 [REDACTED]</p> <p>8 [REDACTED]</p> <p>9 [REDACTED]</p> <p>10 A Well, it was -- it was -- I was interested in</p> <p>11 Dr. Annavaram's opinion that there was actual RTL</p> <p>12 provided by Nuvia that ended up in Arm offerings.</p> <p>13 So --</p> <p>14 Q You're talking about in the counterclaims? The</p> <p>15 CMN?</p> <p>16 A Let me think a minute. Yes, that's where it</p> <p>17 is. There was some -- there was some email that I saw</p> <p>18 that he was citing to that he thought justified that</p> <p>19 summary.</p> <p>20 Q Separate from the counterclaims -- because</p> <p>21 you're right; it did come up there.</p> <p>22 [REDACTED]</p> <p>23 [REDACTED]</p> <p>24 [REDACTED]</p> <p>25 [REDACTED]</p>

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1 A No. Well, I don't remember doing that. I
2 remember focusing only on the other direction.

[illegible]

Page 216

[illegible]

Page 215

[illegible]

Page 217

[illegible]

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1 March 2021."

2 Do you see that at the top?

3 A Yes.

4 Q And then, less than a year later, in February

5 of 2022, [REDACTED]

6 [REDACTED]

7 [REDACTED]

8 Do you see that?

9 A Yes.

10 Q What is your understanding of what is a green

11 signal?

12 A What the design team wanted to know was [REDACTED]

13 [REDACTED]

14 [REDACTED]

15 [REDACTED]

16 [REDACTED]

17 [REDACTED]

18 [REDACTED]

19 [REDACTED]

20 [REDACTED]

21 [REDACTED]

22 [REDACTED]

23 Q And the green signal comes from Arm -- right?

24 -- to Qualcomm?

25 A Yeah, it was an implied judgment call by them

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1 that [REDACTED]

2 [REDACTED].

3 Q Okay. And this was done through [REDACTED]

4 [REDACTED]

5 A Yes, yes.

6 Q Okay. And the submission for the green signal,

7 do you understand that that was done under the Qualcomm

8 ALA credentials?

9 MR. MUINO: Objection. Form.

10 THE WITNESS: I -- well, they couldn't -- Nuvia

11 didn't exist anymore, so they couldn't have done it --

12 I'm not sure what it means to submit under credentials.

13 Is that -- I'll take your representation if

14 that's what Arm calls it. But I know that, you know, you

15 have to be a licensee or you better not send them a

16 database expecting them to do anything with it. They're

17 not a customer of mine.

18 But they were a customer. They were a

19 licensee. And it was -- it was Qualcomm that submitted

20 it at the time -- at this time that resulted in the green

21 signal.

22 BY MS. NYARADY:

23 Q And Qualcomm submitted it under its own ALA.

24 Are you aware of that?

25 MR. MUINO: Objection. Calls for -- sorry.

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1 Objection. Calls for a legal conclusion.

2 THE WITNESS: Yeah, I don't know the

3 ramifications of -- of -- I just -- I just think in terms

4 of the chips.

5 BY MS. NYARADY:

6 Q Okay. I mean, if you don't know, that's fine

7 too.

8 But I mean, do you know one way or the other

9 whether the submission that led to this green signal was

10 under the Qualcomm ALA or the Nuvia ALA?

11 A Yeah, no, I don't.

12 Q Okay. At this point in time, in February

13 of 2022, the Nuvia ALA had not yet been

14 terminated; correct?

15 A It was terminated in March of 2022?

16 Q Correct.

17 A Okay. So yeah -- so no, it had not yet been

18 terminated.

19 Q Okay. And then you go on to say that in April

20 of 2022, [REDACTED]

21 [REDACTED] correct?

22 A Yes.

23 Q And by April of 2022, the Nuvia ALA had been

24 terminated; correct?

25 A Yes. The month before, I think.

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1 Q And so are you aware that --

2 Or do you know whether [REDACTED]

3 [REDACTED]

4 MR. MUINO: Objection. Calls for a legal

5 conclusion.

6 THE WITNESS: I -- I don't know. I remember

7 wondering when I first ran into the timing of this how

8 that worked out with terminating one license but, yet,

9 still, obviously, working on it in terms of figuring out

10 whether it complies.

11 BY MS. NYARADY:

12 Q Were you wondering why Arm would be confirming

13 compliance of a product if there had been a termination

14 of the Nuvia ALA and if there was a suspicion or

15 allegation that the product they were approving was, in

16 fact, stemming from the Nuvia work?

17 MR. MUINO: Objection. Form.

18 THE WITNESS: Yeah, partly that. And, partly,

19 just I know how companies work, especially big companies.

20 The left hand and the right hand don't always communicate

21 with each other.

22 And I just kind of was looking for is there

23 some aspect of this timing that related to that. I don't

24 think I saw one. But -- and I also didn't know whether

25 Arm was somehow contractually obligated to [REDACTED]

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1 that same thing for the same fundamental reasons. So I
2 simply assume that. I mean, I did note that this is a
3 judgment experience based on kind of a notion, but I'm
4 confident in it.

5 Q So I mean, it would be best practice to do
6 that?

7 A I would go so far as to say it's only practice.
8 You don't get this wrong.

9 Q Yeah, I mean, except what about -- we talked a
10 little bit about how sometimes things operate a little
11 differently in the start-up world.

12 I mean, it's possible -- isn't it? -- just
13 resource-wise and whatnot that maybe it didn't run that
14 smoothly in the case of Nuvia?

15 A Yeah, but even in those cases, I can't see the
16 team moving forward. Yeah, I think one could argue --
17 this is what I remember from our earlier discussion.

18 One could argue that perhaps the start-up team
19 wouldn't have had the resources to do as much testing of
20 their own, for example.

21 But if they run the ACK against some feature in
22 the chip that should have worked, they can't move
23 forward. There's no better time.

24 Q Did you review the deposition transcript of
25 Jignesh Trivedi?

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<p style="text-align: right;">Page 230</p> <p>1 A Yes.</p> <p>2 [REDACTED]</p> <p>3 [REDACTED]</p> <p>4 [REDACTED]</p> <p>5 [REDACTED]</p> <p>6 [REDACTED]</p> <p>7 [REDACTED]</p> <p>8 [REDACTED]</p> <p>9 [REDACTED]</p> <p>10 [REDACTED]</p> <p>11 [REDACTED]</p> <p>12 [REDACTED]</p> <p>13 [REDACTED]</p> <p>14 [REDACTED]</p> <p>15 [REDACTED]</p> <p>16 [REDACTED]</p> <p>17 [REDACTED]</p> <p>18 [REDACTED]</p> <p>19 [REDACTED]</p> <p>20 [REDACTED]</p> <p>21 [REDACTED]</p> <p>22 [REDACTED]</p> <p>23 [REDACTED]</p> <p>24 [REDACTED]</p> <p>25 [REDACTED]</p>	<p style="text-align: right;">Page 232</p> <p>[REDACTED]</p> <p>[REDACTED]</p> <p>[REDACTED]</p> <p>[REDACTED]</p> <p>7 Q Okay. I want to talk a little bit about</p> <p>8 Dr. Chen's analysis that you have stated that you are in</p> <p>9 agreement with.</p> <p>10 And it's fair to say -- right? -- that you</p> <p>11 relied on Dr. Chen's analysis in your report?</p> <p>12 A I did.</p> <p>13 Q Okay. First of all, he uses the terms</p> <p>14 "significant" and "substantial" when referring to the</p> <p>15 analysis at times.</p> <p>16 Is there any difference between those two</p> <p>17 words, in your mind?</p> <p>18 A I would have to see specifically how he used</p> <p>19 them to answer that.</p> <p>20 Q Well, if they're being used in the same context</p> <p>21 to describe the amount of overlapping code, in that</p> <p>22 nature, is there a difference, in your mind, as to what</p> <p>23 is meant to be significant RTL code or substantial RTL</p> <p>24 code?</p> <p>25 To be clear, I'm not trying to trick you. I</p>
<p style="text-align: right;">Page 231</p> <p>[REDACTED]</p> <p>2 [REDACTED]</p> <p>3 [REDACTED]</p> <p>4 [REDACTED]</p> <p>5 [REDACTED]</p> <p>6 [REDACTED]</p> <p>7 [REDACTED]</p> <p>8 [REDACTED]</p> <p>9 [REDACTED]</p> <p>10 [REDACTED]</p> <p>11 [REDACTED]</p> <p>12 [REDACTED]</p> <p>13 [REDACTED]</p> <p>14 [REDACTED]</p> <p>15 [REDACTED]</p> <p>16 [REDACTED]</p> <p>17 [REDACTED]</p> <p>18 [REDACTED]</p> <p>19 [REDACTED]</p> <p>20 [REDACTED]</p> <p>21 [REDACTED]</p> <p>22 [REDACTED]</p> <p>23 [REDACTED]</p> <p>24 [REDACTED]</p> <p>25 [REDACTED]</p>	<p style="text-align: right;">Page 233</p> <p>1 asked him the same question. And my recollection is he</p> <p>2 said he didn't mean anything different.</p> <p>3 A I believe --</p> <p>4 Q I just -- I just want to make sure that</p> <p>5 somehow, you know, you're not --</p> <p>6 A Yeah, I'm going down a different path</p> <p>7 thinking -- I can think of cases where those words can be</p> <p>8 used in different ways and you can't substitute them.</p> <p>9 But I can think of other cases where they are</p> <p>10 synonymous.</p> <p>11 Q When you're talking about the core-to-core</p> <p>12 comparison, which is the quantitative analysis that he</p> <p>13 did that you also discuss in your report.</p> <p>14 A Yeah.</p> <p>15 Q I mean, if you use the word "significant" or</p> <p>16 "substantial," would you mean anything different?</p> <p>17 A I would not. The ordering in my brain is if</p> <p>18 you find substantial similarity, that's significant.</p> <p>19 Q Okay. So what is -- what would be substantial</p> <p>20 similarity, in your mind?</p> <p>21 A Anything that isn't -- that couldn't -- I'm not</p> <p>22 sure how to say this. It is -- it is possible but</p> <p>23 unlikely that two random pieces of RTL might have a code</p> <p>24 line in them that is identical.</p> <p>25 It can happen. It's not common, though,</p>

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<p style="text-align: right;">Page 234</p> <p>1 because signal names are usually pretty unique. And they 2 appear in different places. And there's comments 3 sometimes that sort of would also differentiate one line 4 from another. 5 So but still, if it was just one line out of a 6 thousand-line program, you might look at it and say that 7 could just be strictly a coincidence and doesn't mean 8 anything. But if you find that half of the lines in the 9 code or even 20 or 30 percent, that's very unlikely. 10 I mean, I don't -- statistically, that just 11 seems -- that boggles my mind to consider that that might 12 be some kind of cosmic coincidence. 13 Q And that's true even if the same coder for 14 both -- for similar purposes? 15 A For small amount of code, it wouldn't surprise 16 me if the coder's individual style might cause certain 17 lines to look more similar than they would have 18 otherwise. 19 But we're not talking about a couple hundred 20 lines of code here. There were thousands and thousands 21 of lines. 22 Q And so you said 20 to 30 percent even you think 23 would be substantial. 24 Is that fair? 25 A I did say that. I think it's true. We could</p>	<p style="text-align: right;">Page 236</p> <p>1 analogies. And that's the one that jumped to my mind. 2 Maybe that's a soft problem and we can import the 3 solution. I don't know. 4 Q You know we're all going to run out and go 5 research this after this deposition; right? 6 A Maybe I will too. I don't know. 7 Q I don't know the answer. 8 Do you know or do you understand that [REDACTED] 9 and [REDACTED] three of the Qualcomm custom cores or custom 10 core products, have both midsize and large cores? 11 Are you aware of that? 12 A I remember at least one of those did. I -- I 13 don't remember off the top of my head that all three do. 14 Q With respect to -- and, again, I'm not -- in an 15 effort to be transparent, I asked Dr. Chen this. He said 16 that no analysis was done of the midsize cores in those 17 products; that the only -- the chart that you-all did and 18 that are in his report were only of the large cores. 19 Do you have any reason to dispute that? 20 A Not sitting here at the moment, no. 21 Q Okay. What do you know about the differences 22 between the Arm v8 architecture and the v9 architecture? 23 A I remember reading the v9 architecture manual 24 at some point because I was just curious. But I don't 25 remember exactly off the top of my head, no, I don't</p>
<p style="text-align: right;">Page 235</p> <p>1 argue about ten percent or some lower number than that, 2 but. 3 Q So is there a hard cutoff? 4 A I don't think so. It's one of those "you know 5 it when you see it" kinds of things. This can't be a 6 coincidence. There's a connection between those two 7 things. 8 Q So there is at least a range where it becomes 9 subjective. 10 Would you agree with me? 11 A In effect, I think there is just because it's 12 hard to quantify this thing. I would not be surprised to 13 find out -- and you may know the answer to this -- were 14 there's laws associated with plagiarism. How do they 15 handle this? It's roughly the same thing. 16 If I publish a book that has a million lines in 17 it and I stole 50 of them and they were -- you know, is 18 that plagiarism by the law? I don't actually know. 19 I know that there's a fair use doctrine and 20 things like that, but the details are lost. 21 Q You're not accusing Qualcomm of stealing 22 anything, are you? 23 A Heck no. I respect Qualcomm. 24 Q Just checking. 25 A No, I'm just -- I like to think in terms of</p>	<p style="text-align: right;">Page 237</p> <p>1 remember. 2 Q Do you have any sense of the magnitude of 3 changes that would be necessary to -- instead of going, 4 for example, from 8.5 to 8.6 to 8.7 to go and then start, 5 you know, v9, what -- what kind of changes, if you know, 6 would be required to, kind of, jump to the intersection 7 version of Arm architecture? 8 A Yeah, if I could recall what I read about v9, I 9 could answer that, but I don't. I did walk away from 10 that little interloop with the impression that v9 was a 11 reasonably large step. 12 But that's -- that's all I can remember right 13 now. 14 Q The fact that some of the Qualcomm custom cores 15 are v9, does that impact at all your opinion as to 16 whether or not those cores would be derivative of the [REDACTED] 17 [REDACTED] that is v8? 18 A No. 19 Q Why not? If it's a substantial change to go to 20 v9 and to have a product that is v9 compliant versus v8 21 compliant? 22 A Well, the way I'm looking at it is, the 23 v9-compliant core is also compatible with v8. And so all 24 of that stuff that was already derivative, they just 25 added something on top of it that didn't fundamentally</p>

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<p style="text-align: right;">Page 266</p> <p>1 Did the lawyers give you an electronic copy of 2 what they produced? There's a lot of rules under the 3 protective order of what you're allowed to do with the 4 code. 5 A Yeah, I understand. I did say Control F 6 search. That would imply online, but I don't remember. 7 Q Okay. In the materials considered, when you 8 list the code base, where did you review the code base? 9 That was in Palo Alto? You went to Palo Alto for that? 10 A Yeah, I'm spacing out. If I did go to Palo 11 Alto, I'm not remembering it. What I remember is looking 12 at papers, source code printed on papers, and looking 13 through that. 14 My best recollection, sitting here now, is that 15 that's where this list came from. 16 MS. NYARADY: Did the -- Counsel, I ask that 17 anything that he was given be produced to us. 18 BY MS. NYARADY: 19 Q Do you remember the volume of source code that 20 was provided to you -- 21 A Like how many pages? 22 Q Huh? 23 A Like how many pages or? 24 Q Yeah. Because my understanding from 25 Dr. Annavaram is that these code bases that you list here</p>	<p style="text-align: right;">Page 268</p> <p>1 were referring to something beyond that? 2 A That would be a logical inference, but I just 3 -- I can't agree to it now. I just don't remember. 4 Q You don't recall looking at the full CMN code 5 bases? 6 A That's for sure. I don't remember that. 7 Q Okay. 8 MS. NYARADY: All right. Why don't we take a 9 quick break. 10 THE VIDEOGRAPHER: The time is 5:39 p.m. Off 11 record. 12 (Break held off the record.) 13 THE VIDEOGRAPHER: The time is 5:54 p.m. We're 14 back on record. 15 MS. NYARADY: And I have no further questions. 16 Thank you very much for your time, Dr. Colwell. 17 MR. MUINO: I'd like to take just a few minutes 18 just to see if I have any questions. Let's take five 19 minutes. 20 THE VIDEOGRAPHER: The time is 5:55 p.m. We're 21 off record. 22 (Break held off the record.) 23 THE VIDEOGRAPHER: The time is 6:02 p.m. We're 24 back on record. 25 MR. MUINO: So I'd like to designate the whole</p>
<p style="text-align: right;">Page 267</p> <p>1 in the materials considered are quite voluminous. 2 A Yeah. 3 Q I wouldn't think they would be printed out and 4 given to you. But -- 5 A No -- no, so nobody sent me a mountain of 6 source code. I would remember that. 7 Q Okay. 8 A And I don't think I went and looked at it 9 online. I think what I was provided was the pieces that 10 Dr. Annavaram was -- was pointing too. 11 And those are the ones I searched at and looked 12 at and said, "I don't see it." 13 Q Okay. Do you know why all of the code bases 14 are listed in the materials considered if you didn't look 15 at them? 16 A Well, I did look at the pieces. 17 Q The pieces that you did? 18 A I didn't look at all of them, yeah. 19 Q Okay. Because that's also separately listed. 20 A Oh, which is? 21 Q I believe at the bottom of "Produced Materials" 22 where it says, "ARM_SC_2, and then it's got numbers 1 23 through 49. I believe those are the actual printouts for 24 Dr. Annavaram. 25 So I thought when you listed code bases, you</p>	<p style="text-align: right;">Page 269</p> <p>1 transcript highly confidential under the protective 2 order. 3 Dr. Colwell, I have no questions for you. 4 THE VIDEOGRAPHER: The time is 6:02 p.m. Off 5 record. 6 (At 6:02 p.m., the deposition of 7 DR. ROBERT COLWELL was adjourned.) 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25</p>

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1 DECLARATION UNDER PENALTY OF PERJURY
2
3 I, DR. ROBERT COLWELL, do hereby certify under
4 penalty of perjury that I have reviewed the foregoing
5 transcript of my deposition taken on June 28, 2024; that
6 I have made such corrections as appear noted herein in
7 ink; that my testimony as contained herein, as corrected,
8 is true and correct.

10 DATED this ____ day of _____,
11 20____, at _____, California.

DR. ROBERT COLWELL

ERRATA SHEET
VERITEXT/NEW YORK REPORTING, LLC

CASE NAME: Arm Ltd. v. Qualcomm Inc., Et Al.
DATE OF DEPOSITION: 6/28/2024
WITNESSES' NAME: Robert Colwell

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Robert Colwell

SUBSCRIBED AND SWORN TO BEFORE ME
THIS ____ DAY OF _____, 20__.

(NOTARY PUBLIC) MY COMMISSION EXPIRES: _____

REPORTER'S CERTIFICATION

3 I, Desiree Cooks, Certified Shorthand Reporter in
4 and for the State of California, do hereby certify:

6 That the foregoing witness was by me duly sworn;
7 that the deposition was then taken before me at the time
8 and place herein set forth; that the testimony and
9 proceedings were reported stenographically by me and
10 later transcribed into typewriting under my direction;
11 that the foregoing is a true record of the testimony and
12 proceedings taken at that time.

13 Further, that if the foregoing pertains to the
14 original transcript of a deposition in a federal case,
15 before completion of the proceedings, review of the
16 transcript [] was [] was not requested.

18 IN WITNESS WHEREOF, I have subscribed my name on
19 this date: July 3, 2024

DmC

Desiree Cooks, CSR No. 14075

EXHIBIT 27

EXHIBIT 28

EXHIBIT 29

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IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

ARM LTD.,

Plaintiff,

v.

QUALCOMM INC., QUALCOMM
TECHNOLOGIES, INC. and NUVIA, INC.,

Defendants

C.A. No. 22-1146 (MN)

**OPENING EXPERT REPORT OF DR. MURALI ANNAVARAM
REGARDING QUALCOMM’S COUNTERCLAIM**

May 20, 2024

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I. INTRODUCTION

1. My name is Murali Annavaram. I have been retained as an expert in this action on behalf of Defendants Qualcomm Inc., Qualcomm Technologies (collectively, “Qualcomm”), and Nuvia, Inc. (“Nuvia”) (together, “Defendants”). My qualifications are set forth in my previously-submitted expert report in this matter on December 20, 2023 (“Opening Report”), which I incorporate by reference in its entirety in this report. As with my Opening Report, my Rebuttal Report dated February 27, 2024, and my Reply Report dated March 25, 2024, are each incorporated by reference in this Report (my “Counterclaim Opening Report”). I am being compensated for my work on this case at my standard consulting rate of \$600 per hour. I am also being reimbursed for expenses that I may incur. My compensation is not contingent upon the results of my analysis or the substance of my opinions or testimony.

2. I expect to be called to provide expert testimony regarding opinions formed resulting from my analysis of the issues considered in this Counterclaim Opening Report, the materials that I have relied upon, and how I reached my opinions. If asked to testify about these issues, I may also discuss my own work, teaching, and publications in the field, knowledge of the state of the art in the relevant time period, and what certain technical terms are understood to mean in the field, including by those involved in the design of microarchitectures. I may rely on handbooks, textbooks, technical literature, my own personal experience in the field, and other relevant materials and/or information to explain relevant technologies, the state of the art in the relevant period, and the development of relevant technologies. I may also create demonstratives to further explain some of the discussion that appears in this report. And, I may also discuss the source code that Qualcomm and/or ARM LTD. (“ARM”) has made available for inspection that I have personally reviewed many times.

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3. I reserve the right to modify or supplement my opinions, as well as the basis for my opinions, in light of new positions taken by ARM or its experts, the nature and content of the documentation, data, proof, and other evidence or testimony that Plaintiff, ARM, or its experts may present, or any additional discovery or other information provided to me or found by me in connection with this matter.

4. I reserve the right to supplement the opinions in this Report if any subsequent testimony or facts are revealed through discovery, as well as if any subsequent reports are produced by ARM’s experts.

II. SUMMARY OF OPINIONS

5. I have been informed that Nuvia provided Confidential Information to ARM, requesting that ARM include certain features in ARM’s Coherent Mesh Network (“CMN”) products.¹ I understand that the parties agree that ARM implemented many of the features that Nuvia requested. A subset of these requested features are specifically referred to as [REDACTED]

[REDACTED]
[REDACTED] (collectively the “Identified Features”). For this Report, I have been asked to analyze materials regarding the Identified Features, including ARM’s produced source code (the “ARM CMN Codebases”) relating to the Identified Features, and offer my expert opinions as to whether ARM’s CMN Products implement the Identified Features.

¹ See, e.g., QCARM_7643686; QCARM_3862422; QCARM_3862424; QCARM_7643929; QCARM_7634057.

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6. I have also been informed that in certain instances, Nuvia provided ARM with changes to the CMN register transfer language (“RTL”). During my review, [REDACTED]

7. I have not evaluated the significance of the features requested by Nuvia with respect to the performance or functionality of the CMN Products, or as compared to other features present in the CMN Products, as I understand that ARM has not produced documents sufficient to show which features were developed independently by ARM, which features were requested by other of ARM’s partners, or that show the research and development efforts and activities related to the CMN Products. I reserve the right to supplement this Report should ARM produce additional, relevant documents.

8. I submit this Report to describe my opinions related to the inclusion of the Identified Features in ARM’s CMN Products. A description of some of the materials reviewed appears in Section III. For background, I provide a technology overview of interconnection networks and ARM’s CMN in Section IV. For additional background, I refer to my Opening Report and Rebuttal Report dated December 20, 2023 and February 27, 2024, respectively, which I incorporated by reference in this Report. In Section V, I generally describe the functionality of each of the Identified Features, and I identify locations in the ARM CMN Codebases where the implementations for each Identified Feature are found. Finally, in Section VI, I identify the presence of Nuvia Contributed Source Code in certain ARM CMN Products.

9. It is my opinion, based on my expertise in processor design and my review of ARM’s CMN Codebases, that each of the Identified Features except [REDACTED] [REDACTED] are implemented in certain ARM CMN Products that I will refer to as the “Affected CMN Products,” including at least [REDACTED]

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[REDACTED], that the [REDACTED] feature appears in at least some of the Affected CMN Products, and that the Affected CMN Products also include Nuvia Contributed Source Code. I provide more detailed analysis of my findings in Section V (regarding the Identified Features) and Section VI (regarding the Nuvia Contributed Source Code) of this Report.

III. BASIS FOR OPINIONS

10. My opinions are made in view of my knowledge and experience in the technical areas at issue in this Report and the materials that I have considered.

11. As part of my preparation for writing this Report, I reviewed the materials listed in Appendix A to this Report. These materials include, but are not limited to, the following: (1) ARM's CMN source code (in ARM's CMN Codebases), (2) ARM's technical manuals for the ARM CMN Products, and (3) discovery responses and deposition transcripts. Regarding CMN source code, I was provided access to and have reviewed source code for the following CMN products in the ARM CMN Codebases:

[illegible]

IV. TECHNOLOGY BACKGROUND

A. Overview of Mesh Networks

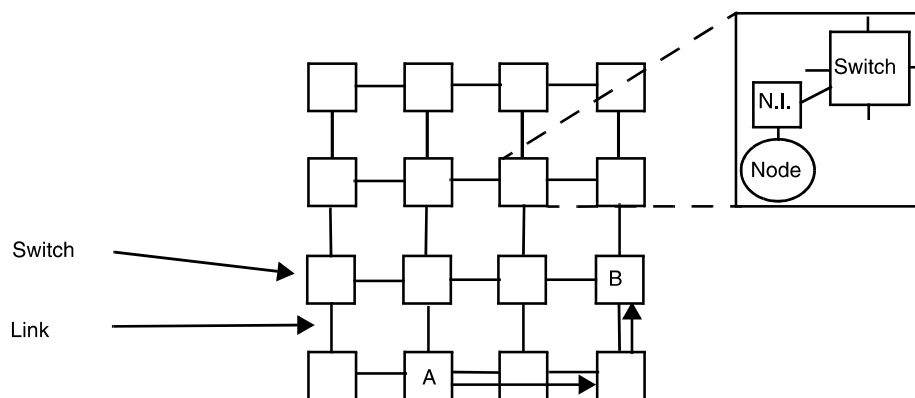
12. Chip Multiprocessors (CMPs) are a common processor design in which multiple cores are constructed on a single chip (sometimes referred to as a single die, which is a single piece of semiconductor material such as Silicon). When integrating multiple cores on a single chip there

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is a need to allow these cores to communicate with each other, with other memory structures on the chip, and with other input/output (“I/O”) components on the chip. For example, each of the cores may benefit from accessing memory components shared by all of the cores, including a system level cache (“SLC”) and a last level cache (“LLC”). This communication capability is provided by an on-chip interconnection network, also called a network-on-chip (“NoC”). NoCs are a common component of CMPs. Design choices for NOCs are made based, in part, on the amount of data to be communicated between the cores and the amount of data to be communicated between the cores and memory. Designers may make choices to achieve maximum performance of the cores while abiding by power limitations on the chip. Poor design choices in the NoCs can create bottlenecks in the communication paths that reduce the performance of the cores. For example, performance may be lost when the CMP cannot exploit thread-level parallelisms across processor cores. The design choices made for NoCs thus have an impact on performance of CMPs.

13. NoCs can be designed according to one of many topologies. An example of a simple NoC includes a single bus that couples all the cores and SLC/LLC memories to the bus. A bus is a single contention-based communication medium. When one core sends data, that core takes exclusivity of the bus. Accordingly, single-bus NoCs are difficult to scale.

14. Another example NOC topology includes parallel communication paths, such as a mesh network. An example mesh network is shown below:



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Dubois, Michel, Murali Annavaram, and Per Stenström. *Parallel computer organization and design*. Cambridge University Press, 2012.

15. The mesh illustrated above has a 4-by-4 topology, with 16 switches organized into 4 rows with 4 columns. A switch is also referred to as a mesh cross-point (“MXP”). Each MXP is connected to, at most, four neighbouring MXPs in a mesh network. The four neighbouring MXPs of an MXP are to the right, left, bottom, and top of the current cross-point. Each MXP is connected to each neighbouring MXP using a link, which is one or more wires that can transfer digital information between an output port of one switch and an input port of another. Each MXP can also connect to one node (e.g., a processor core, a slice of SLC/LLC memory, or other interfacing devices).

16. In a mesh design, when two nodes communicate, the transmitted data may traverse links that are shared by more than one MXP. When data moves through a shared link, there can be contention between competing nodes attempting to transmit data over the same link. To resolve contention, switches may implement a variety of techniques including: buffering information, hand shake mechanisms, or credit tokens. The credit token technique, for example, involves assigning a certain number of credits to a node connected to a particular MXP. When that node transmits a message over that MXP, the node uses up one of its assigned credits. The node may recover credits when messages are delivered to the corresponding destination node.

17. A mesh network communicates data by splitting the data into small portions called message packets. For example, a node may request cached data from the SLC. Such a request is followed by a response from the SLC node that directs the cache data to be filled back into the requesting node’s local cache from the SLC and through the mesh. The size of the data communicated can exceed the buffer capacity of an MXP in the mesh. For example, a node (e.g.,

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a core) may request data from the SLC that results in data exceeding the MXP buffer capacity. The mesh network splits the data into fixed-size packets to communicate the data in smaller portions that fit the MXP buffer capacity. In some cases, a packet may be further split into fixed-size chunks called flits.

B. Background of ARM’s CMN

18. ARM offers products that include interconnection networks called “CMN Products.” ARM’s CMN Products implement the mesh topology that I describe above. ARM’s CMN Products include multiple versions released over the years, including, but not limited to, CMN-600, Neoverse CMN-700 Max, and, most recently, CMN-Cyprus-Max.

V. CERTAIN OF ARM’S CMN PRODUCTS INCORPORATE THE IDENTIFIED FEATURES

19. It is my opinion, based on my review of the considered materials, including the ARM CMN Codebases, that each of the Identified Features are implemented in at least [REDACTED] [REDACTED] and [REDACTED] [REDACTED] (together, these versions of the [REDACTED] are the “Affected CMN Products”). In the following sections, I provide an overview of each Identified Feature followed by, when applicable, my analysis of where in ARM’s CMN Codebases an Identified Feature is implemented.²

² I have printed source code files demonstrating the implementation of these features from the representative versions of source code produced by ARM. *See* ARM_SC_2_00000001 – 103. I also cite to specific files below in the course of my analysis of the Identified Features. I reserve the right to testify regarding any portion of the ARM CMN Codebases, without restriction to the portions of source code that I printed.

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A. [REDACTED]

20. I have been informed that one of the Identified Features is [REDACTED] In [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

21. I understand ARM admitted in its response to Qualcomm’s Interrogatory No. 27 that [REDACTED]

[REDACTED]. I have reviewed the produced code and also identified the [REDACTED] feature present in the ARM CMN Codebases for the Affected CMN Products.

22. Based on my review of the ARM CMN Codebases, I have confirmed that the Affected CMN Products include [REDACTED], which is implemented at least in the [REDACTED]

[REDACTED]

[REDACTED]

23. As an example, if [REDACTED] is enabled then [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

³ <https://developer.arm.com/documentation/102308/0300/?lang=en> (§ 3.1.1.14.1)

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24. As another example, [REDACTED] defines a [REDACTED]

[REDACTED]
[REDACTED]
[REDACTED]

25. As another example, the [REDACTED]

[REDACTED]
[REDACTED]
[REDACTED]
[REDACTED]

26. While I provided some example code locations of this feature and its uses in the ARM CMN Codebases corresponding to [REDACTED], I have also verified that [REDACTED]

[REDACTED].

27. I also verified that [REDACTED] was not implemented in earlier versions of the ARM CMN Products and is not present in ARM CMN Codebases corresponding to [REDACTED]

[REDACTED]

B. [REDACTED]

28. I have been informed that another of the Identified Features is [REDACTED]

[REDACTED]
[REDACTED]
[REDACTED]

29. I understand that ARM admitted in its response to Qualcomm’s Interrogatory No. 27 that [REDACTED] is implemented at least in [REDACTED] (corresponding to product

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██████████ I have reviewed the produced code and also identified the ██████████ feature present in the ARM CMN Codebases for the Affected CMN Products.

30. Based on my review of the ARM CMN Codebases, I confirmed that the Affected CMN Products include [REDACTED], which is implemented in the [REDACTED] product [REDACTED] [REDACTED]. As an example, [REDACTED]

31. While I provided some example code locations of this feature and its uses in the ARM CMN Codebases corresponding to [REDACTED], [REDACTED] is implemented in [REDACTED]

32. I also verified that [REDACTED] was not implemented in earlier versions of the ARM CMN Products and is not present in ARM CMN Codebases corresponding to [REDACTED]

C. [REDACTED]

33. I have been informed that another of the Identified Features is [REDACTED]

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[REDACTED]

34. I understand ARM admitted in its response to Qualcomm’s Interrogatory No. 27 that [REDACTED] is implemented at least in [REDACTED] (corresponding to product [REDACTED]). I have reviewed the produced code and also identified the [REDACTED] feature present in the ARM CMN Codebases for the Affected CMN Products.

35. Based on my review of the ARM CMN Codebases, I confirmed that the Affected CMN Products include [REDACTED], which is implemented at least in the [REDACTED] product in [REDACTED]. As an example, [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

36. While I provided some example code locations of this feature and its uses in the ARM CMN Codebases corresponding to [REDACTED], I have also verified that [REDACTED] is implemented in [REDACTED]

37. I also verified that [REDACTED] was not implemented in earlier versions of the ARM CMN Products and is not present in ARM CMN Codebases corresponding to [REDACTED]

[REDACTED]

⁴ <https://developer.arm.com/documentation/102308/0300/?lang=en> (§ 3.9.8)

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D.

38. I have been informed that another of the Identified Features is

includes

39. I understand ARM admitted in its response to Qualcomm's Interrogatory No. 27 that the [REDACTED] feature is implemented at least in [REDACTED] (corresponding to product [REDACTED]). I have reviewed the produced code and also identified the [REDACTED] feature present in the ARM CMN Codebases for the Affected CMN Products.

40. Based on my review of the ARM CMN Codebases, I confirmed that the Affected CMN Products include [REDACTED], which is implemented at least in the [REDACTED] product in [REDACTED]

As an example,

⁵ <https://developer.arm.com/documentation/102308/0300/?lang=en> (§ 7.2)

⁶ <https://developer.arm.com/documentation/102308/0300/?lang=en> (§ 3.3)

⁷ <https://developer.arm.com/documentation/102308/0300/?lang=en> (§ 3.3.8)

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[REDACTED]

[REDACTED] [REDACTED] [REDACTED] [REDACTED] [REDACTED] [REDACTED] [REDACTED] [REDACTED] [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

41. In [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

42. While I provided some example code locations of this feature and its uses in the [REDACTED] product, I have also verified that [REDACTED] is implemented [REDACTED]

43. I also verified that [REDACTED] was not implemented in earlier versions of the ARM CMN Products and is not present in ARM CMN Codebases corresponding to [REDACTED]

E. [REDACTED]

44. I have been informed that another of the Identified Features is [REDACTED] By default, the CMN checks the SLC for all requests targeting memory, even if the request was a non-cacheable or no-snoop request type. On a hit, the request is completed in the SLC instead of being forwarded to the memory controller. When enabled, [REDACTED]

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[REDACTED]

[REDACTED]

45. I understand ARM admitted in its response to Qualcomm’s Interrogatory No. 27 that the [REDACTED] feature is implemented at least in [REDACTED] (corresponding to product [REDACTED]. I have reviewed the produced code and also identified the [REDACTED] feature present in the ARM CMN Codebases for the Affected CMN Products.

46. Based on my review of the ARM CMN Codebases, I confirmed that the Affected CMN Products include the [REDACTED] feature, which is implemented at least in the [REDACTED] product in [REDACTED]

As an example, [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

⁸ <https://developer.arm.com/documentation/102308/0300/?lang=en> (§ 3.9.9)

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47. As yet another example, [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

48. Similarly, when [REDACTED] is enabled, [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

49. While I provided some example code locations of this feature and its uses in the [REDACTED] product, I have also verified that [REDACTED] is implemented in [REDACTED]

50. As one example, [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

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51. I also verified that [REDACTED] was not implemented in the other ARM CMN Products and is not present in ARM CMN Codebases corresponding to [REDACTED]

F. [REDACTED]

52. I have been informed that another of the Identified Features is [REDACTED]. By default, the CMN has the ability to decode a portion of the system address map to target CMN internal configuration registers.⁹ This requires that the system address maps for each RNI, Distributed Virtual Memory (“DVM”) Request Node (“RND”), Fully coherent Request Node (“RNF”), and mesh interconnect be configured to forward that region to the DVM Home Node (“HND”). When the HND detects that a request from a request node (e.g., RNI, RND, or RNF) matches the correct region it forwards the request to its internal network that handles configuration register accesses. Additionally, the HND provides an Advanced Peripheral Bus (“APB”) target such that external components may drive configuration register accesses directly to the same internal network.¹⁰ [REDACTED]

[REDACTED]¹¹

53. I understand ARM admitted in its response to Qualcomm’s Interrogatory No. 27 that the [REDACTED] feature is implemented at least in [REDACTED] (corresponding to product [REDACTED]).

⁹ <https://developer.arm.com/documentation/102308/0300/?lang=en> (§ 3.1.1.10)

¹⁰ <https://developer.arm.com/documentation/102308/0300/?lang=en> (§ 4.1.1)

¹¹ <https://developer.arm.com/documentation/102308/0300/?lang=en> (§ 4.1.6)

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VI. CERTAIN OF ARM’S CMN PRODUCTS INCORPORATE RTL PROVIDED BY NUVIA

54. I understand that prior to the acquisition in the context of discussions regarding Nuvia’s requested features, Nuvia provided ARM with proposed changes to the CMN RTL.

55. I have reviewed one such communication sent on December 2, 2020 from Nuvia to ARM in which [REDACTED]

[REDACTED]

56. I have identified the same lines of RTL provided in the communication, the Nuvia Contributed Source Code, in the ARM CMN Codebases corresponding to the Affected CMN Products [REDACTED] ARM_SC_2_00000104 – 263.

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VII. RESERVATION OF RIGHTS

57. My opinions are subject to change according to additional opinions that ARM’s experts may present and information I may receive in the future or additional work I may perform. With this in mind, I reached the conclusions and opinions in this Report.

58. At trial and as discussed above, I may rely on visual aids and may rely on analogies concerning any related technologies.

59. In connection with my anticipated testimony in this action, I may use as exhibits various documents produced in this case that refer or relate to the matters discussed in this Report. I have not yet selected the particular exhibits that might be used. In addition, I may create or assist in the creation of certain demonstrative evidence to assist me in testifying, and I reserve the right to do so.

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I certify under penalty of perjury that the foregoing is true and correct.

Date: May 20, 2024

A handwritten signature in blue ink, appearing to read 'Murali', is positioned above a horizontal line.

Murali Annavaram, Ph.D.

Los Angeles, California

EXPERT REPORT OF MURALI ANNAVARAM CONTAINS CONFIDENTIAL BUSINESS
INFORMATION SUBJECT TO PROTECTIVE ORDER

APPENDIX A

MATERIALS CONSIDERED

1. Documents referenced in my Opening Expert Report regarding Qualcomm's Counterclaims.

2. Discovery Responses and witness deposition transcripts, including:

2024.05.10 – ARM's Supplemental R&Os to Qualcomm's ROGs 26-28
2024.05.10 – Larri, Guy Deposition Transcript
2024.05.16 – Vedaraman, Geetha Deposition Transcript

3. Produced Documents

ARM_01456132
QCARM_7643686
QCARM_3862422
QCARM_3862424
QCARM_7643929
QCARM_7634057
ARM_SC_2_00000001 – 263

4. Publicly Available Materials

Dubois, Michel, Murali Annavaram, and Per Stenström. <i>Parallel computer organization and design</i> . Cambridge University Press, 2012.
Arm Neoverse CMN-700 Coherent Mesh Network Technical Reference Manual Revision r3p0 https://developer.arm.com/documentation/102308/0300/?lang=en (last visited May 20, 2024)
Arm Neoverse CMN-700 Coherent Mesh Network Technical Reference Manual Revision r3p2 https://developer.arm.com/documentation/102308/0302/?lang=en (last visited May 20, 2024)
Arm CoreLink MMU-700 System Memory Management Unit Technical Reference Manual Revision r0p1 https://developer.arm.com/documentation/101542/0001/?lang=en (last visited May 20, 2024)

5. [REDACTED]

[REDACTED]	[REDACTED]	[REDACTED]	[REDACTED]
[REDACTED]	[REDACTED]	[REDACTED]	[REDACTED]
[REDACTED]	[REDACTED]	[REDACTED]	[REDACTED]
[REDACTED]	[REDACTED]	[REDACTED]	[REDACTED]

EXPERT REPORT OF MURALI ANNAVARAM CONTAINS CONFIDENTIAL BUSINESS
INFORMATION SUBJECT TO PROTECTIVE ORDER

	[REDACTED]
	[REDACTED]
	[REDACTED]
	[REDACTED]
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	[REDACTED]
[REDACTED]	[REDACTED]
	[REDACTED]
	[REDACTED]
	[REDACTED]
[REDACTED]	[REDACTED]
	[REDACTED]
	[REDACTED]
	[REDACTED]
	[REDACTED]
	[REDACTED]
	[REDACTED]
	[REDACTED]

EXHIBIT 30

**IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE**

ARM LTD., a U.K. corporation,
Plaintiff,

v.

QUALCOMM INC., a Delaware
corporation, QUALCOMM
TECHNOLOGIES, INC., a
Delaware corporation, and NUVIA,
INC., a Delaware corporation,
Defendants.

C.A. No. 22-1146 (MN)

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**REBUTTAL EXPERT REPORT OF DR. ROBERT P. COLWELL TO
DR. ANNAVARAM’S OPENING EXPERT REPORT REGARDING
QUALCOMM’S COUNTERCLAIM**

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I. INTRODUCTION

1. My name is Dr. Robert P. Colwell, and I have been retained as an expert witness on behalf of the Plaintiff Arm Ltd. in the case captioned *Arm Ltd. v. Qualcomm Inc. et al.*, No. 1-22-cv-001146MN (D. Del.). I am being compensated for my time in connection with this proceeding at \$650/hour. My compensation is not dependent on the substance of my opinions, my testimony, or the outcome of this proceeding.

2. I have been asked to review and respond to the Opening Expert Report of Dr. Murali Annavaram Regarding Qualcomm's Counterclaim ("Annavaram Counterclaim Report" or "Annavaram Count. Rep."), dated May 20, 2024, and materials Dr. Annavaram cited and considered. I may adjust or supplement my opinions as appropriate based on Dr. Annavaram's reply to this rebuttal report or new information.

3. Dr. Annavaram provides opinions regarding certain features in Arm's Coherent Mesh Network ("CMN") products.¹ Specifically, Dr. Annavaram addresses six features that Nuvia asked Arm to implement in the CMN products: [REDACTED]

¹ Annavaram Counterclaim Report at ¶ 5

[REDACTED]

[REDACTED]² Dr. Annavaram refers to these six features as the “Identified Features.”³ Dr. Annavaram opines that the Identified Features, except for [REDACTED], are implemented in [REDACTED] (collectively, the “Relevant CMN Products”).⁴ Dr. Annavaram also opines that RTL provided by Nuvia was incorporated into Arm’s CMN codebases.⁵

4. As discussed in this report, it is my opinion that the Identified Features, which were only six features out of thousands contained in the Relevant CMN Products, (1) are minor adjustments to existing features previously developed by Arm, (2) have limited use cases, and/or (3) were known to engineers developing Networks-on-Chip (defined below) before Nuvia proposed the features to Arm. From my review of the materials cited by Dr. Annavaram, I see no evidence that any Nuvia RTL was incorporated into Arm’s CMN code, and I am not aware of any such evidence.

5. I base my opinions on my extensive experience in the industry; experience with Arm technology; my review of the materials cited by Dr. Annavaram in his report; my review of deposition transcripts; my review of discovery responses; a conversation I had with Arm fellow Mark Werkheiser

² *Id.*

³ *Id.*

⁴ *Id.* at ¶¶ 8-9.

⁵ *Id.* at ¶¶ 54-56.

on May 31, 2024; and other materials. I include a list of materials considered in Appendix A to this report.

II. EXPERIENCE AND QUALIFICATIONS

6. My qualifications are summarized in Section II of my Opening Expert Report (“Colwell Report” or “Colwell Rep.”), submitted in this matter on December 20, 2023.

III. FACTUAL BACKGROUND

A. Arm’s Coherent Mesh Network (CMN)

1. Network-on-Chip

a. Background

7. Modern general purpose programmable integrated circuits comprise dozens of functional units such as processors, GPUs, interfaces to various I/O standards like USB and PCIe, image processing accelerators, multiple radio protocols, memory controllers, and power controllers. Such an integrated circuit is generally known as a System-on-Chip (SoC). All of the functional units within an SoC need to communicate with system main memory, as well as each other. In the much simpler systems of the past, these communications would have been achieved by a shared bus. Today’s complex designs, however, require much higher performance than a shared bus can achieve. These complex designs take advantage of the several-orders-of-magnitude higher transistor counts and signal path availability afforded by silicon chip integration. Thus, many of the communication systems in today’s SoCs are achieved via modern on-chip interconnect

facilities known as Network-On-Chip (NoC), which inherits many concepts from the large-scale networks of the past.

8. The general purpose of a NoC is to connect memories, processors, and other functional units of an SoC so that they can communicate with each other. In doing so, the NoC coordinates and routes data traffic in the SoC, resolves potential communication conflicts, and, if it is a cache coherent NoC, ensures cache coherency within the system.

9. As an example, if a processor in an SoC wants to read a particular piece of data from main memory, the request must traverse the NoC to get from the processor to main memory. Likewise, the response from main memory must traverse the NoC in the reverse direction to get back to the processor. The NoC efficiently routes the request and response and resolves any shared-resource conflicts that may occur. In this example, the processor is the initiator of the request and main memory is the target of the request.

(i) Unidirectional Communication Path

10. As mentioned above, the simpler systems of the past used shared buses for communication. Shared buses are bi-directional, i.e., data may flow in either direction on the bus wires. When wires were expensive and scarce, this was an efficient scheme. But when a bus “changes direction,” for electrical reasons, the bus generally cannot carry traffic for one clock cycle during the changeover. The loading and inevitable electrical stubs of a

shared bus also generally impose an upper limit on how fast the bus can be clocked.

11. Modern NoCs, however, split interconnect transactions into request/response pairs, such that any given network transfer is unidirectional. For example, a direct link between two components A and B will be composed of two wires – one for data going from A to B, and another for data going from B to A. Wires are no longer efficiently shared, but on a silicon chip, wires are (relatively) inexpensive. The lost turnaround clock cycle is avoided, and the clock can be made much faster.

(ii) Competing Influences

12. SoC designers procure or design the various functional units included in their chip. They juggle a large number of competing influences: more and faster functional units mean higher performance (in general), but also higher cost in die area, licensing expenses, and power; new IP blocks can help the chip be competitive, but they also represent higher product risk given the designers' limited experience with them; being on the same die, the highly complex digital circuits in the processors and accelerators may interact electrically with the sensitive analog circuits in the wireless functional units, such as Bluetooth and Wi-Fi.

13. Similarly, competing influences also impact NoC designs. There are tradeoffs, for example, between performance, power, size, and complexity.

14. Competing influences also impact NoCs in another way – all functional units compete for shared resources such as main memory access

and shared links in the NoC, and managing such competing accesses is a primary task for the shared NoC interconnect.

b. NoC Considerations

15. Interconnect designs can be acquired via licensed IP blocks. Companies such as Arm, Sonics, and Arteris offer NoC “products”; companies such as TI and Intel have their own NoC designs.

16. When designing or purchasing NoCs, companies must consider several factors such as size, performance, scalability, power, cache coherence, error detection and handling, and configuration.

(i) Size

17. The various interconnects vary in the amount of silicon real estate required. Silicon die area is usually a first-order determinant of yield and product cost, so all else being equal, smaller is better.

(ii) Performance

(1) Quality-of-Service (QoS)

18. Quality-of-Service is a catch-all phrase relating to how reliably an interconnect performs and provides its services. Some NoC researchers maintain that QoS necessarily requires a guarantee of performance, not just best-effort.

(2) Priority Schemes

19. Not all traffic traversing the NoC interconnect is equally important. For example, an SoC may have a file transfer occurring between a connected USB device and a wireless link, while the user is watching a

video. If the video data stream briefly falls behind the frame rate, the user may experience lost frames or other undesirable artifacts, but if the file transfer is briefly delayed, the user will not care.

20. Some NoCs have provisions for identifying higher priority traffic which receives preferred handling, at the possible expense of lower priority traffic. For example, some NoCs allow the SoC functional units to tag their transactions with priorities.

(3) Traffic Congestion Detection, Prevention, Handling

21. NoC's are somewhat like the streets of a city. At low traffic conditions, things flow smoothly, and the vehicles on the street experience nominal delays and expected latency/throughput. But at higher traffic conditions, it becomes clear that the vehicles are competing for shared resources and are causing the overall throughput to slow considerably. If the traffic across the NoC is well distributed, with no "hotspots," even a relatively high overall load may be handled well. But if multiple initiators all want the same resource (e.g., main memory), together they can overload various parts of the NoC, and slow each other down to the point where no requests are filled. Some NoCs have explicit provisions for identifying, preventing, and handling traffic congestion.

(4) Deadlocks and Fairness

22. A deadlock occurs when a system makes no further forward progress. A common reason for deadlock is that resources are shared in such

a way that two or more resources are required for a successful transit across the NoC. Initiator X acquires the first resource but fails to acquire the second one because Initiator Y already has it; meanwhile, Y can't proceed because it needs what X has.

23. Fairness is the notion that every task should get its fair share of the system resources. It is acceptable for a low priority task to wait for a higher priority task, but it is unacceptable for that low priority task to fail because it never received data from the shared system resource. Fairness methods ensure that even the lower priority tasks get serviced.

(5) Throughput and Latency

24. Throughput is often the performance metric of choice for NoC vendors. It usually represents the most traffic per unit time that the vendor's NoC can sustain. It is often a formidable number, especially if there are a lot of initiators and targets. In practice, however, the throughput one actually obtains in normal system operation, both average and peak, will be much lower, partly due to non-peak demand, and partly due to various NoC overheads.

25. Latency refers to the time it takes for a request to traverse the NoC. It is a function of the clock rate, the number of registers in the path, and the average contention for shared resources, such as NoC switch output ports.

(iii) Scalability

26. To send a transaction across the NoC, an initiator first conveys the necessary information across its own local interconnect to its Network Interface Unit (NIU, or MXP in Arm CMN parlance), which is its dedicated interface to the NoC. From there, the NIU converts the initiator's request into the data format of the NoC and sends the request on its way. At the far side of the NoC, that request arrives at the target's NIU, and converts from the NoC internal data format to whatever standard is used by the target.

(iv) Power

27. NoCs are generally relatively large, fast components of modern SoCs, and therefore contribute substantially to the power demands (and thermal dissipation) of the systems. Active measures are therefore appropriate for controlling their power usage and, if necessary, throttling them in order to stay within system cooling capabilities or energy usage limits. Clocking flipflops and registers causes them to dissipate power, so gating the clocks to those storage elements during idle cycles is a standard power optimization technique. Monitoring circuits for instantaneous operating temperature is also a common capability and can be used to establish overall power usage in case additional measures are needed.

(v) Cache Coherence

28. Modern processor cores have caches, temporary fast storage that allows the processor to take advantage of common aspects of most code: (a) if

the processor accesses a data item, it will probably do so again (“temporal locality”); and (b) if the processor accesses a data item, it will probably also access other data nearby (“spatial locality”).

29. For maximum performance, a processor may load data from main memory and put it in its local cache. If the processor never changes that data item’s value, there is no cache coherence problem, because the cached value is equal to the value still in main memory.

30. However, if the processor writes to that data item, the cached version of the data will update while the main memory version of the data is not written. At that instant, if another agent in the system accesses the same data item from main memory, it will find a “stale,” version of the data. To avoid this, cache coherent NoCs provide a mechanism by which any such attempts to access a stale copy of data in memory will be prevented, often by a form of overall memory monitoring known as snooping.

31. Modern SoCs and NoCs can be cache coherent or non-cache coherent. As cache coherency and snooping add a layer of complexity, and thus cost, companies may choose non-cache coherent NoCs if cache coherence is not a required feature for the market or industry they occupy.

32. Cache-coherent SoC’s will also often have a provision for making certain memory accesses non-cache-coherent. Such a feature is used when the data being accessed is known to be part of a large data structure that would overflow the cache, or will not be re-accessed.

(vi) Error detection and handling

33. Various system errors can occur in an NoC-based SoC chip. For instance, to minimize battery drain, a power controller on the SoC may power-down a functional unit. If an initiator attempted to access that functional unit via a request across the NoC, the target's NIU might recognize that a system-level error has occurred and return an error indication to the initiator.

2. Arm's CMN Products

34. At least since 2016, Arm has offered CMN products to its licensees, including CMN-600, CMN-600AE, CMN-650, CMN-700, and CMN-Cyprus. CMN stands for Coherent Mesh Network. As the name suggests, the CMN products are cache-coherent NoC interconnects.

35. Arm supports several CMN products for different use cases and market niches. Each CMN product is intricately designed and, according to Mr. Werkheiser, has thousands of features. Arm also routinely adds new features and extensions to its CMN products. The Identified Features cited by Dr. Annavaram, only represent six features out of thousands in just one CMN Product.

36. Below, I provide some information regarding each CMN Product.

a. CMN-600

37. CMN-600 was Arm’s first product in its CMN line, launched in 2016.⁶ “The Arm CoreLink CMN-600 Coherent Mesh Network is designed for intelligent connected systems across a wide range of applications including networking infrastructure, storage, server, HPC, automotive, and industrial solutions. The highly scalable mesh is optimized for Armv8-A processors.”⁷ The CMN-600’s technical reference manual, which “describes the functionality and the effects of functional options on the behavior of CMN-600,” is available online.⁸

b. CMN-600AE

38. CMN-600AE has a more specific scope compared to CMN-600. “The Arm CoreLink CMN-600AE Coherent Mesh Network is designed for high performance automotive systems across a wide range of applications including digital cockpit, advanced driver-assistance systems (ADAS) and autonomous driving systems.”⁹ The CMN-600AE technical reference manual can be found online.¹⁰

⁶ See John De Gelas, *New ARM IP Launched: CMN-600 Interconnect for 128 Cores and DMC-620, an 8Ch DDR4 IMC*, AnandTech (September 27, 2016 11:00 AM EST), <https://www.anandtech.com/show/10711/arm-cmn-600-dmc-620-128-cores-8-channel-ddr4>; Arm CoreLink CMN-600 Coherent Mesh Network Technical Reference Manual (Revision r2p0, 2016-2018), <https://developer.arm.com/documentation/100180/0200>.

⁷ CoreLink Coherent Mesh Network, Arm Limited, <https://www.arm.com/products/silicon-ip-system/corelink-interconnect/cmn-600>.

⁸ Arm CoreLink CMN-600 Coherent Mesh Network Technical Reference Manual, (“CMN-600 Manual”) at § 2.1, <https://developer.arm.com/documentation/100180/0200/bry1434478370033>.

⁹ CoreLink CMN-600AE, <https://developer.arm.com/Processors/CoreLink/CMN-600AE>.

¹⁰ Arm® CoreLink™ CMN-600AE Coherent Mesh Network Technical Reference Manual (“CMN-600AE Manual”) (Revision r1p1, 2019-2023), <https://developer.arm.com/documentation/101408/0101/?lang=en>.

c. CMN-650

39. CMN-650 made several improvements to CMN-600, while still being optimized for Armv8-A processors.¹¹ For example, while CMN-600 supports up to 32 processor compute clusters, CMN-650 supports 256. CMN-650 also supports AMBA CHI Issue D (Advanced Microcontroller Bus Architecture), whereas CMN-600 only supports AMBA CHI Issues B and C.¹² AMBA stands for Advanced Microcontroller Bus Architecture and is Arm’s “freely available, open standard for the connection and management of functional blocks in a . . . SoC.”¹³ “The AMBA CHI (Coherent Hub Interface) specification defines the interfaces for the connection of fully coherent processors.”¹⁴

d. CMN-700

40. “The CMN-700 product is a scalable configurable coherent interconnect that is designed to meet the Power, Performance, and Area (PPA) requirements for Coherent Mesh Network systems that are used in high-end networking and enterprise compute applications.”¹⁵

41. “The basic structure of CMN-700 is a configurable rectangular grid that is composed of network routers that are known as *Crosspoints* (XPs)

¹¹ Arm Neoverse CMN-650 Coherent Mesh Network Technical Reference Manual (“CMN-650 Manual”) at § 2.1 (Revision r2p0, 2019-2021), <https://developer.arm.com/documentation/101481/0200/What-is-CMN-650-/About-CMN-650>.

¹² *Id.*

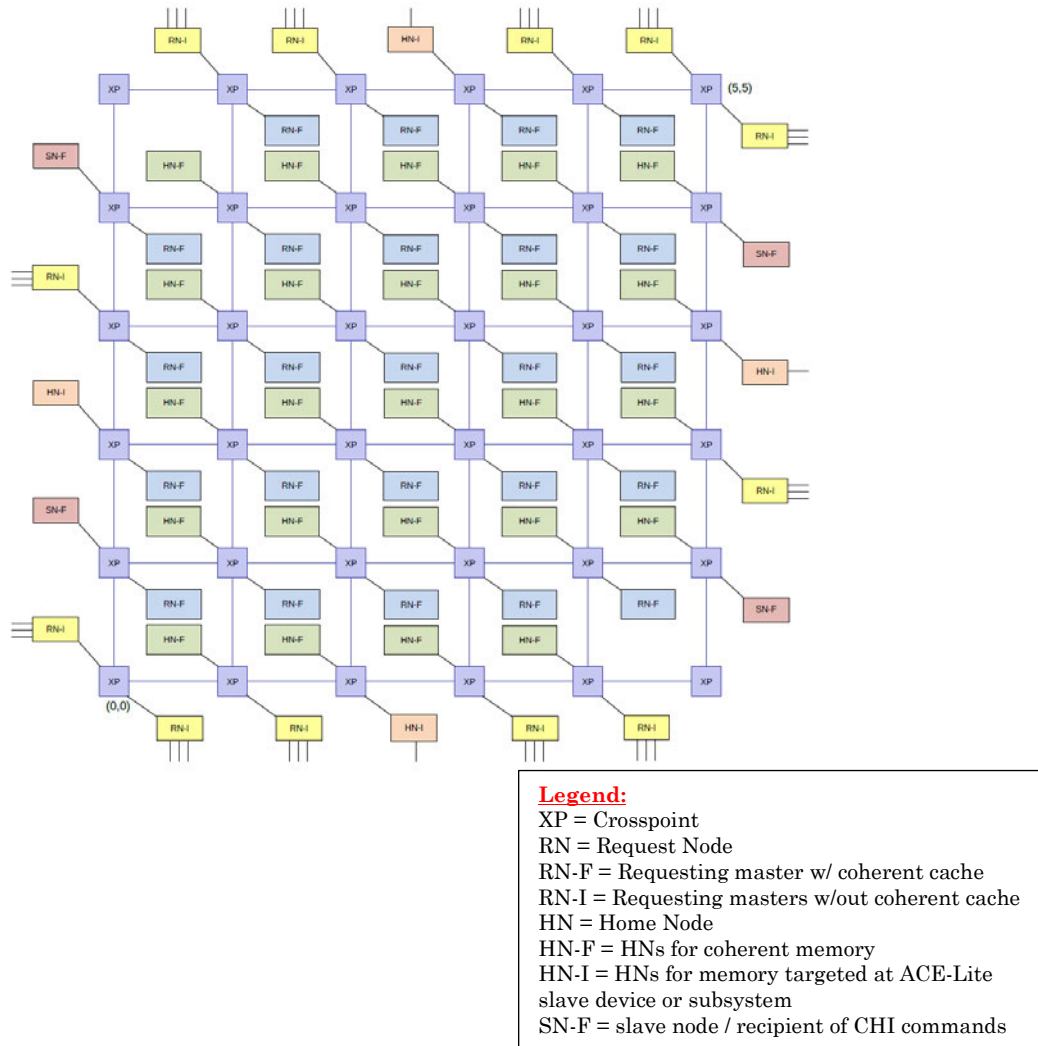
¹³ AMBA CHI Specification, <https://developer.arm.com/Architectures/AMBA>.

¹⁴ *Id.*

¹⁵ Arm Neoverse CMN-700 Coherent Mesh Network, Technical Reference Manual (“CMN-700 Manual”) at § 2.1 (Revision r3p0, 2020-2022), <https://developer.arm.com/documentation/102308/0300/?lang=en>.

and CHI-compliant devices.”¹⁶ “Each XP connects horizontally and vertically to other XPs, creating a two-dimensional mesh structure. In a mesh configuration, each XP can have up to four device ports for connecting CHI-compliant devices.”¹⁷

Figure 3-4: Example 6 × 6 mesh configuration



42. “Request Nodes (RNs) reside outside of the mesh and connect to CMN-700 ports. Requesting masters with coherent caches (processors,

¹⁶ *Id.* § 2.5.

¹⁷ *Id.*

GPUs, or processing elements with internal coherent caches) are referred to as RN-F devices. They connect directly to the CMN-700 interconnect mesh using a CHI RN-F port. I/O-requesting masters without coherent caches connect to CMN-700 RN-I bridge devices using ACE-Lite ports.”¹⁸

43. “In CHI, each byte of address space is assigned to a single *Home Node* (HN). That HN is responsible for handling all memory transactions that are associated with that address.”¹⁹

44. “HN-F device instances are the HNs for all coherent memory. HN-Fs also support noncoherent memory accesses. Memory that is mapped to an HN-F targets DRAM. Each HN-F can contain an SF and an SLC slice. The amount of SLC required determines the number of HN-Fs. The total SLC size required divided by the number of HN-F instances determines the recommended SLC size for each HN-F instance. Generally, each HN-F partition has the same SLC size. The amount of SLC and number of HN-Fs are configured separately.”²⁰

45. “HN-I device instances are the HNs for all memory that targets an ACE-Lite slave device or subsystem. HN-I does not support coherent memory.”²¹

¹⁸ CMN-700 Manual at § 2.5.1.

¹⁹ *Id.*

²⁰ *Id.*

²¹ *Id.*

e. CMN-Cyprus

46. CMN-Cyprus, also known as CMN S3, is Arm’s newest CMN product. It is a “Coherent Mesh Network . . . designed for intelligent connected systems across a wide range of applications, including networking infrastructure, storage, server, HPC, automotive, and industrial solutions. The highly scalable mesh is optimized for Armv9.2, Armv9 and Armv8-A processors, multichip configurations, and CXL attached devices. . . . It can be customized across a wide range of performance points.”²²

47. CMN S3AE has a more specific scope than the general CMN S3. It is a “Highly Scalable Mesh for Large Core Count Automotive Designs Including Chiplets. . . . [It] is designed to enable scalable performance for automotive applications, central compute, and machine learning (ML) workloads.”²³

B. Identified Features

48. Dr. Annavaram specified six features as “Identified Features”:

[REDACTED]

[REDACTED]

[REDACTED]²⁴

49. Although Dr. Annavaram states that “in certain instances, Nuvia provided Arm with changes to the CMN register transfer language

²² Arm Neoverse CMN S3 – Arm®, <https://www.arm.com/products/silicon-ip-system/neoverse-interconnect/cmn-s3>.

²³ *Id.*

²⁴ Annavaram Counterclaim Report at ¶ 5.

(“RTL”),²⁵ Dr. Annavaram does not connect this to any of the Identified Features. Further, Dr. Annavaram fails to clearly identify what RTL supposedly provided by Nuvia to Arm exists in Arm’s CMN codebases, and does not precisely identify the location of such RTL. I address Dr. Annavaram’s 3-paragraph section on Nuvia RTL in § V below.

50. Dr. Annavaram chose not to address the significance of the Identified Features.²⁶ As explained in § IV below, the Identified Features [REDACTED] [REDACTED] Thus, the Identified features have limited value and utility in terms of the overall CMN product. Further, based on my discussion with Mr. Werkheiser, most of the Identified Features were not used by Arm partners other than Nuvia, and [REDACTED] [REDACTED] Some of the features were not even mentioned in the CMN Technical Reference Manuals.

IV. OPINIONS REGARDING THE IDENTIFIED FEATURES

A. [REDACTED]

51. [REDACTED]
[REDACTED]
[REDACTED]
[REDACTED]

²⁵ Annavaram Counterclaim Report at ¶ 6.

²⁶ Annavaram Counterclaim Report at ¶ 7.

²⁷ [REDACTED]

²⁸ [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

52. [REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

53. [REDACTED]

[REDACTED]

[REDACTED]

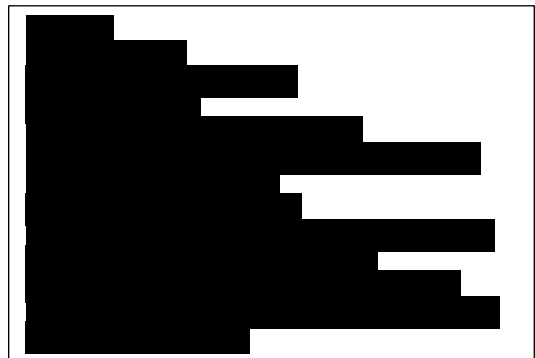
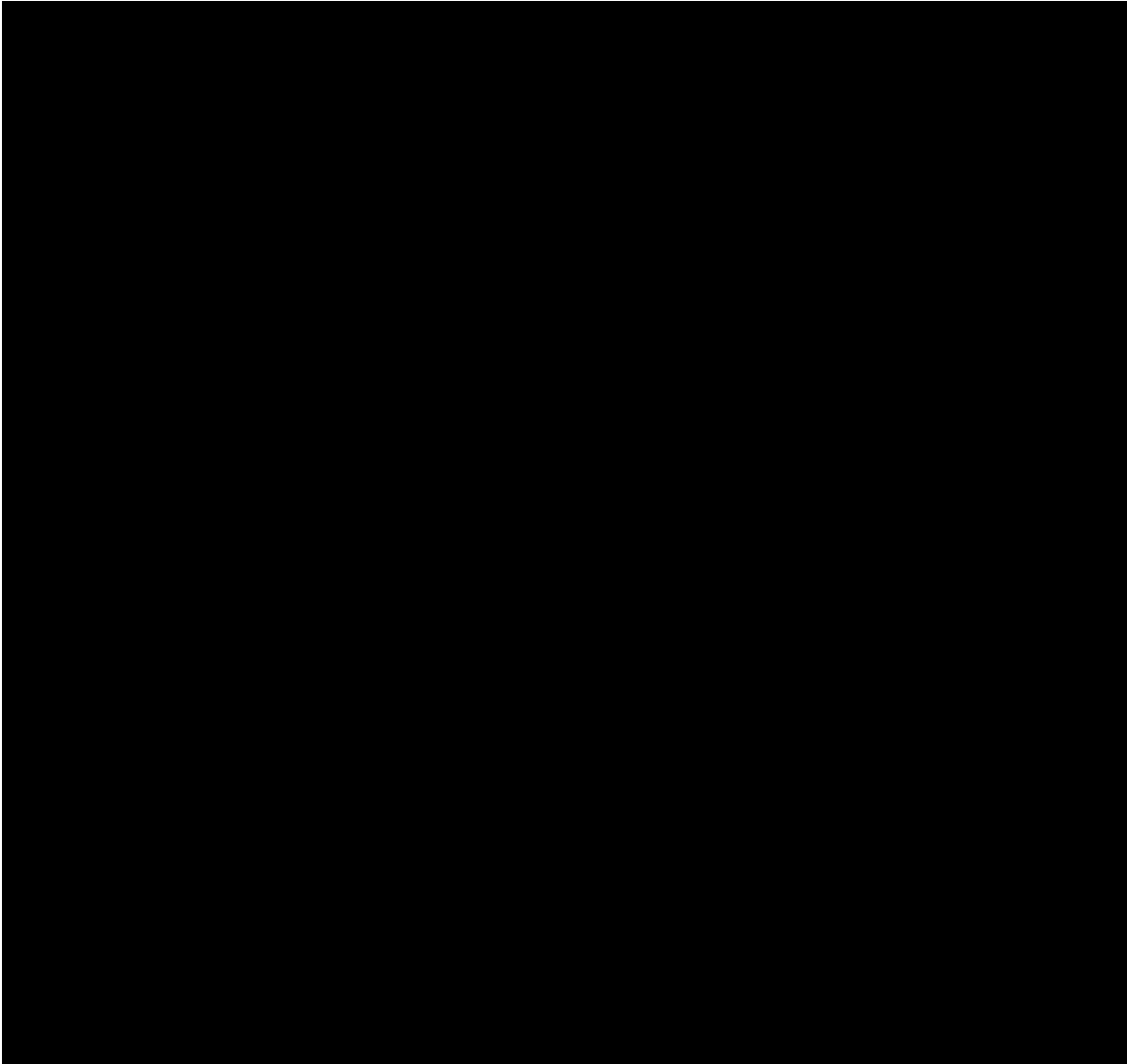
[REDACTED]

[REDACTED]

[REDACTED] [REDACTED]

[REDACTED]

[REDACTED]



54.

[REDACTED]

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57.

[REDACTED]

[REDACTED]

[REDACTED]

██████████

58.

59.

60.

[illegible]

[REDACTED]

[REDACTED]

61. [REDACTED]

[REDACTED]

[REDACTED]

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[REDACTED]

[REDACTED]

62. [REDACTED]

[REDACTED]

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63. [REDACTED]

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The image consists of a single, uniform black rectangle that fills the entire frame. There are no discernible features, text, or patterns other than the solid black color.

[illegible]

A horizontal bar chart titled 'U.S. should take action to address climate change' showing the percentage of respondents who believe the U.S. should take action to address climate change, broken down by age group. The y-axis lists age groups: 18-29, 30-49, 50-64, 65+, and Overall. The x-axis represents the percentage, ranging from 0 to 100. The bars are black. The data is as follows:

Age Group	Percentage
18-29	85%
30-49	95%
50-64	90%
65+	92%
Overall	90%

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

[REDACTED]

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[REDACTED] [REDACTED]

[REDACTED]

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V. DR. ANNAVARAM DOES NOT SUPPORT HIS CLAIM THAT CERTAIN CMN PRODUCTS INCORPORATE NUVIA RTL

116. In the final section of his report, Dr. Annavaram claims that “[c]ertain of Arm’s CMN products incorporate RTL provided by Nuvia.”⁶⁹

117. Dr. Annavaram states that “in the context of discussions regarding Nuvia’s requested [CMN] features, Nuvia provided ARM with proposed changes to the CMN RTL.”⁷⁰ In support, he points to only one

[REDACTED]

⁶⁹ Annavaram Counterclaim Report at § VI.

⁷⁰ Annavaram Counterclaim Report at ¶ 54.

communication – a “December 2, 2020 [email] from Nuvia to Arm in which Nuvia provided recommended alterations to the CMN RTL.”⁷¹

118. Dr. Annavaram states without evidence that he “identified the same lines of RTL provided in the [December 2, 2020 email] in the ARM CMN Codebases corresponding to the Affected CMN Products ([REDACTED] [REDACTED]) [sic]. ARM_SC_2_00000104 – 263.”⁷² While Dr. Annavaram cites to 160 pages of Arm source code, he does not identify or cite to specific portions of the Arm source code where the Nuvia-suggested RTL was allegedly incorporated. In fact, after doing a CTRL+F search on the 160 pages of cited source code, I could not find one instance of the line [REDACTED] – the one Nuvia addition for the [REDACTED].

119. More fundamentally, [REDACTED], the subject of the December 22, 2020 email, is not related to any of the Nuvia-requested features that Dr. Annavaram analyzed. Dr. Annavaram was “asked to analyze materials regarding” [REDACTED]
[REDACTED]
[REDACTED]⁷³ But [REDACTED] is unrelated to these six features. Dr. Annavaram himself does not cite to any [REDACTED] files when analyzing the six identified features.

⁷¹ Annavaram Counterclaim Report at ¶ 55.

⁷² Annavaram Counterclaim Report at ¶ 56.


⁷³ Annavaram Counterclaim Report at ¶ 5.

120. Mr. Werkheiser explained that the [REDACTED] idea relates to implementing the [REDACTED]. [REDACTED]
[REDACTED]
[REDACTED] It is thus unclear why [REDACTED] was included at the end, except as a misguided attempt by Dr. Annavaram to show that Arm utilized Nuvia RTL in its CMN products.

VI. CONCLUSION

121. My opinions above are based on available information to date. I reserve the right to supplement or amend my opinions in this report, and also to rebut opinions by Qualcomm's experts with which I disagree. I also reserve the right to correct any clerical errors that I discover after service of this report.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct. Executed on this 10th day of June of 2024.

By:  _____

Dr. Robert P. Colwell

APPENDIX A
LIST OF MATERIALS CONSIDERED

All documents cited within this report.

Opening Expert Report of Dr. Murali Annavaram Regarding Qualcomm's Counterclaim and documents referenced therein.

PLEADINGS

Arm Ltd. v. Qualcomm Inc. et al., No. 1-22-cv-001146 MN (D. Del.):

ECF No. 300, SEALED Defendant's Answer and Defenses to Plaintiff's Complaint and Jury Demand and Defendants' Second Amended Counterclaims dated March 13, 2024.

ECF No. 318, SEALED Plaintiff Arm Ltd.'s Answer and Affirmative Defenses to Defendants Qualcomm Inc., Qualcomm technologies, Inc., and And Nuvia, Inc.'s Second Amended Counterclaims, dated April 4, 2024.

DISCOVERY

Arm's Supplemental R&Os to Qualcomm's ROGs 26-28, dated May 10, 2024.

DEPOSITION TRANSCRIPTS REVIEWED⁷⁴

Larri Deposition Transcript dated May 10, 2024.

Vedaraman Deposition Transcript dated May 16, 2024.

PRODUCED MATERIALS

ARM_01435488

ARM_01437291

ARM_01437760

ARM_01437793-96

ARM_01437821

ARM_01456132

QCARM_7643686

QCARM_3862422

QCARM_3862424

QCARM_7643929

QCARM_7634057

ARM_SC_2_00000001 – 349

⁷⁴ I had all deposition transcripts available to me.

PUBLICLY AVAILABLE SOURCES

Dubois, Michel, Murali Annavaram, and Per Stenström. Parallel computer organization and design. Cambridge University Press, 2012.

Arm Neoverse CMN-700 Coherent Mesh Network Technical Reference Manual Revision r3p0, <https://developer.arm.com/documentation/102308/0300/?lang=en> (last visited June 9, 2024).

Arm Neoverse CMN-700 Coherent Mesh Network Technical Reference Manual Revision r3p2, <https://developer.arm.com/documentation/102308/0302/?lang=en> (last visited June 9, 2024).

Arm CoreLink MMU-700 System Memory Management Unit Technical Reference Manual Revision r0p1, <https://developer.arm.com/documentation/101542/0001/?lang=en> (last visited June 9, 2024).

John De Gelas, *New ARM IP Launched: CMN-600 Interconnect for 128 Cores and DMC-620, an 8Ch DDR4 IMC*, AnandTech (September 27, 2016 11:00 AM EST), <https://www.anandtech.com/show/10711/arm-cmn-600-dmc-620-128-cores-8-channel-ddr4> (last visited June 9, 2024).

Arm CoreLink CMN-600 Coherent Mesh Network Technical Reference Manual (Revision r2p0, 2016-2018), <https://developer.arm.com/documentation/100180/0200> (last visited June 9, 2024).

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Arm® CoreLink™ CMN-600AE Coherent Mesh Network Technical Reference Manual Revision r1p1, <https://developer.arm.com/documentation/101408/0101/?lang=en> (last visited June 9, 2024).

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AMBA, <https://developer.arm.com/Architectures/AMBA> (last visited June 9, 2024).

Arm Interconnect CMN S3, <https://www.arm.com/products/silicon-ip-system/neoverse-interconnect/cmn-s3> (last visited June 9, 2024).

Arm Cortext-A76 Core Technical Reference Manual Version 0401, <https://developer.arm.com/documentation/100798/0401/smf1554201061027> (last visited June 9, 2024).

ARM CMN CODEBASES

[REDACTED]

